National Cheng-Kung University
Department of Mechanical Engineering
Introduction To Microelectronics Fabrication Process

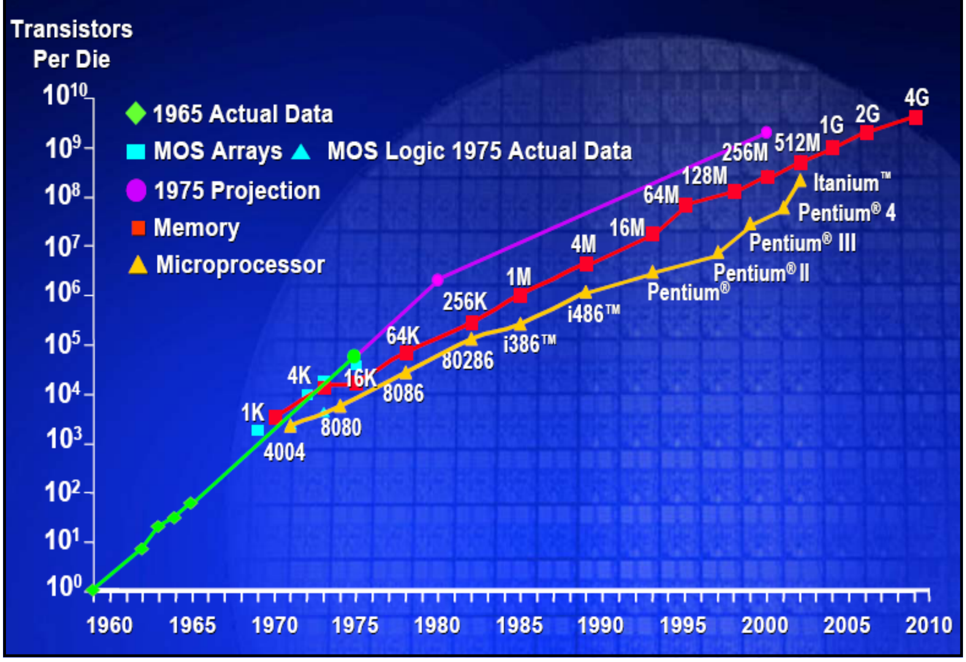
Course Overview and Chapter 1

Kuo-Shen Chen
Sept. 05, 2022

Attention Please!

- This course deals with SMALL stuff
- This course deals with practical issues
- This course uses most of your learned ME knowledge
- This course may not have as many mathematics as other courses
- 這是少數幾門學校教的落後產業發展課程的其中之一

Integrated Circuit Complexity



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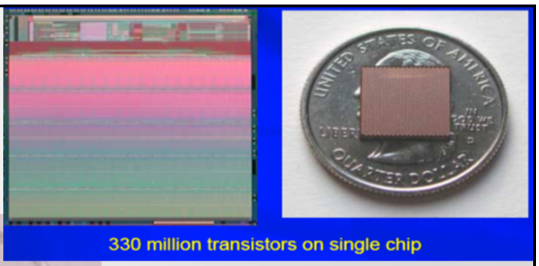
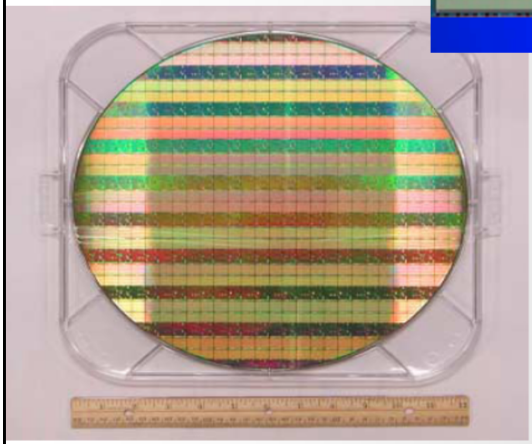
52 Mbit SRAM 90 nm process



330 million transistors on single chip



Total 120 billon transistors

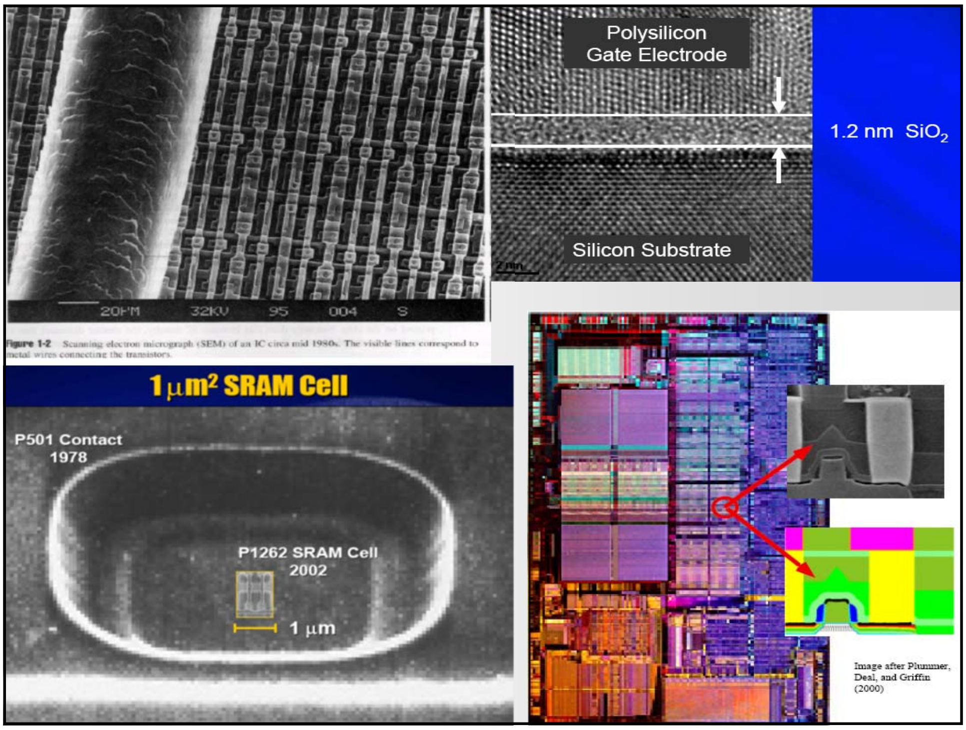


Figure 1-2 Scanning electron micrograph (SEM) of an IC circa mid 1980s. The visible lines correspond to metal wires connecting the transistors.

Image after Plummer, Deal, and Griffin (2000)

半導體工業

- 半導體為我國最具競爭力與重要產值的主要工業
  - 電腦晶片, 記憶體, 邏輯晶片, 類比 IC, 微感測器....
  - 竹科, 南科, 中科 ...
- 衍生產業
  - 電路設計, 設備製造, 原料供應, 封裝, 測試
- 從業人員包含電機, 材料, 機械, 化工, 化學, 物理.....

對於未來生涯規劃, 各位的憧憬是甚麼?

- 錢多, 事少, 離家近?
- 小確性?
- And anything else ....

2015 7th 兩岸實驗力學研討會

- 7/28, 2015 重慶
- 大陸代表 18人, 台灣代表 16人
- 機械/航空領域
- 大陸研究內容:
  - 軌道列車, 衛星結構, 核能安全, 橋樑監控, 智能汽車, 超導力學
- 台灣呢?

Cont'd

- 台灣研究內容:
  - 以顯示器, 電子封裝, 微機電等領域為應用之論文佔 70% 以上

成大機械系畢業生出路統計

- (up to 2019)
- 58% 最後在廣義半導體光電產業工作
- 不管你喜不喜歡, 似乎都要嚴肅面對此事實

Part I:課程相關事項

課程目標與先修科目

- 本課程完全不討論電路設計, 僅就如何製作積體電路之方法與過程進行介紹與說明
- 建議先修科目:
  - 電子電路: 需具備簡單之電工/電子之基礎, 如電阻電容, RC 電路, 半導體特性, 電晶體等知識
  - 機械材料: 具備簡單材料冶金知識
  - 普通化學: 化學反應
  - 材料力學: 簡單之應力/應變知識

Disciplines

ECE

- Electrical Design
- Electrostatic Field Control
- Electrical behavior and limits of materials and material systems
- Using defects for our electrical advantage
- Effects of strain and stress on device reliability
- Designing a better device, circuit, system

Material Science

- Structural Classification of Materials: Crystal Structure
- Formation and control of defects, impurity diffusion
- Strain and Stresses materials
- Materials interactions (alloys, annealing)
- Phase transformations

Chemistry

- Bonding Classification of Materials
- Etching and deposition chemistry
- Chemical cleaning

Physics

- Quantum transport
- Solid state descriptions of carrier motion

Mechanical Engineering

- Heat transfer
- Micro-machines-Micro Electro-Mechanical Machines (MEMS)
- Fatigue/fracture, (especially for packaging) etc...
- Mechanical stresses during processing (polishing, thermal cycles, etc…)

Disciplines

ECE

- Electrical Design
- Electrostatic Field Control

Interested in the uses of these processes

stress on device reliability

- Designing a better device, circuit, system

Material Science

- Str
Clas
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Structure
- Formation and control of defects, impurity diffusion
- Strain and Stresses materials
- Materials interactions (alloys, annealing)
- Phase transformations

Chemistry

- Bonding

deposition chemistry

- Chemical cleaning

Physics

- Quantum transport

Interested in the fundamental process

Mechanical Engineering

- Heat
- Micr ro-
Mech S)
- Fatig for
packa
- Mec rocessing
(polishing, thermal cycles, etc…)

Interested in the uses of these processes

課程展望

After taking this course, you will be able to

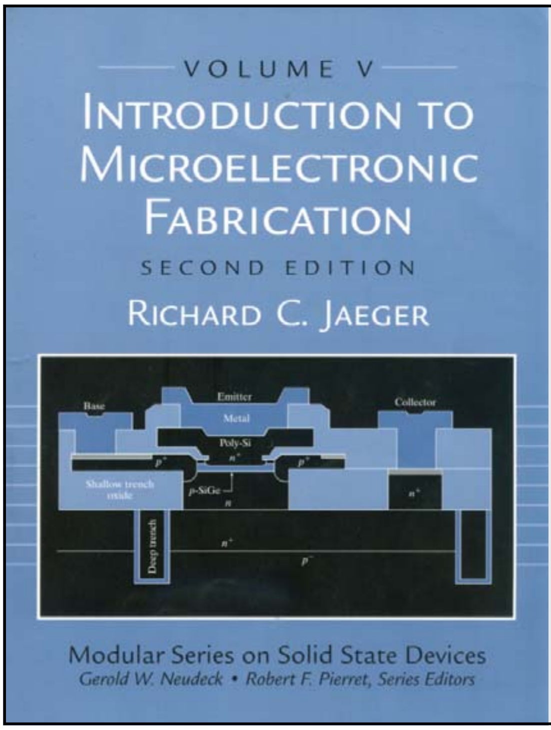
- Use common semiconductor terminology
- Describe a basic IC fabrication sequence
- Briefly explain each process step
- Relate your job or products to semiconductor manufacturing process

Courses after this course

- Semiconductor fabrication related courses
- MEMS related courses
- nanosystems related courses
- semiconductor processes

This Course Has NO Textbooks

- Use course handout as the major materials for preparation
  - Lecture slides
  - Contents copied from books
- However, you should have at least one of the following major references
  - This is extremely important



VOLUME V

INTRODUCTION TO MICROELECTRONIC FABRICATION

SECOND EDITION

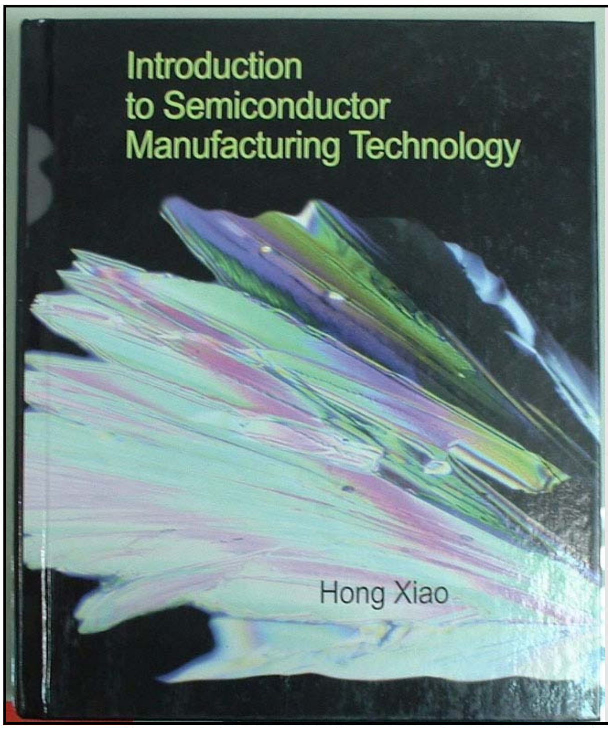
RICHARD C. JAEGER

Modular Series on Solid State Devices

Gerold W. Neudeck • Robert F. Pierret, Series Editors

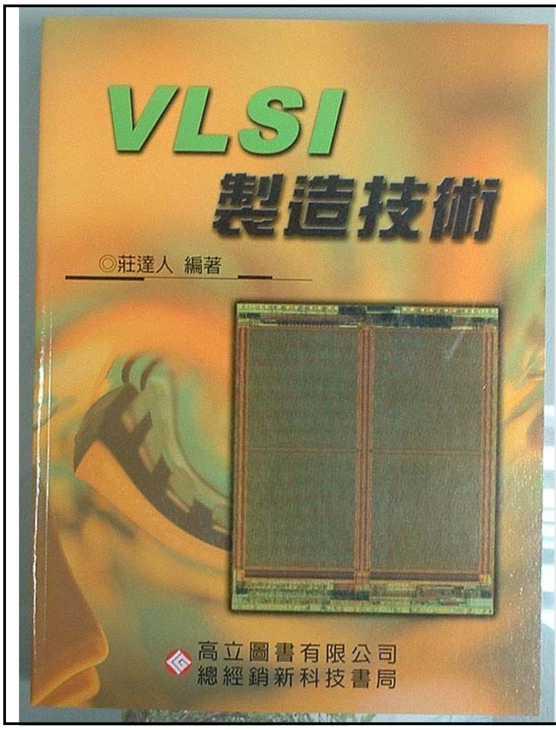
Major reference

- R. C. Jeager, Introduction to Microelectronic Fabrication



Major Reference

- Xiao, Introduction to Semiconductor manufacturing Technology

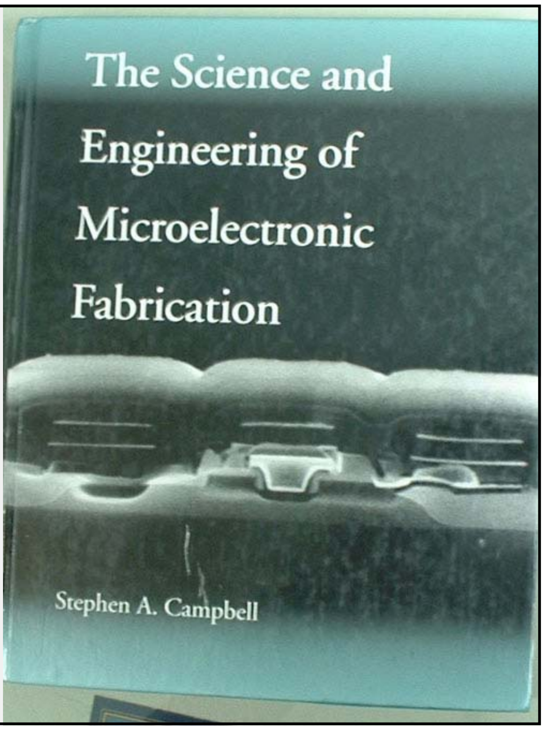


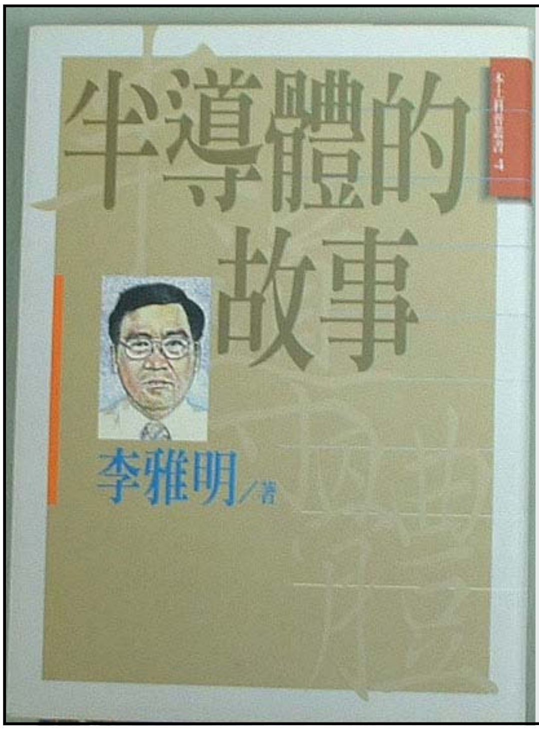
Major Reference

- 莊達人
- VLSI 製造技術

Major Reference

- S. A Campbell, The Science and Engineering of Microelectronic fabrication

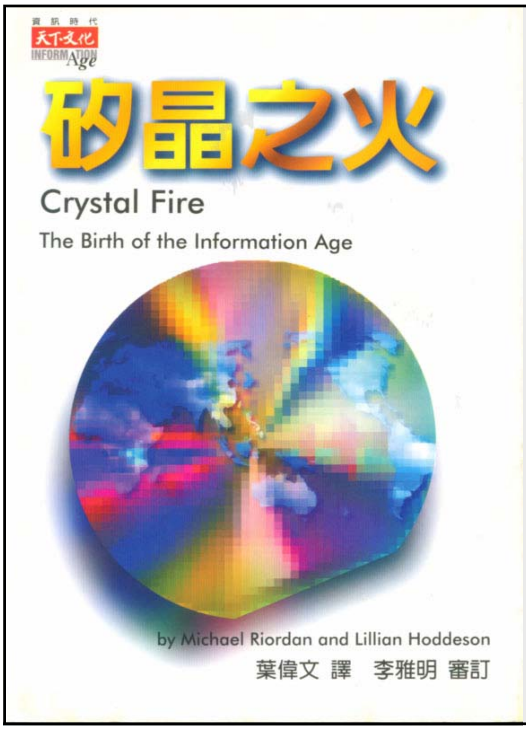




強力推薦

- 李雅明
- 半導體的故事

- (科普)



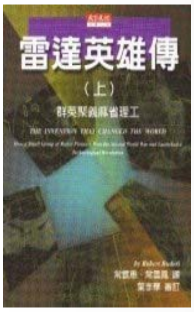
強力推薦

- Crystal Fire

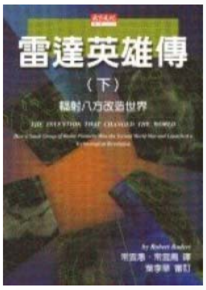
雷達英雄傳

The Invention that Changed the World

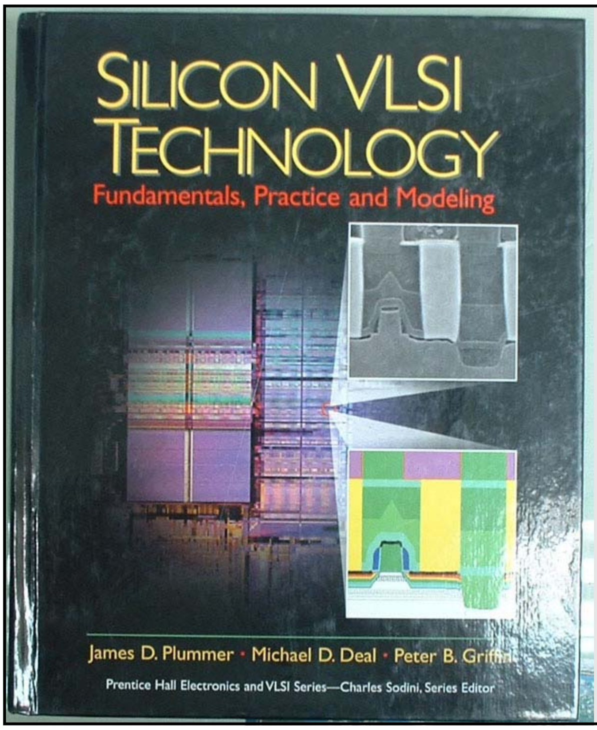
by R. Buderi



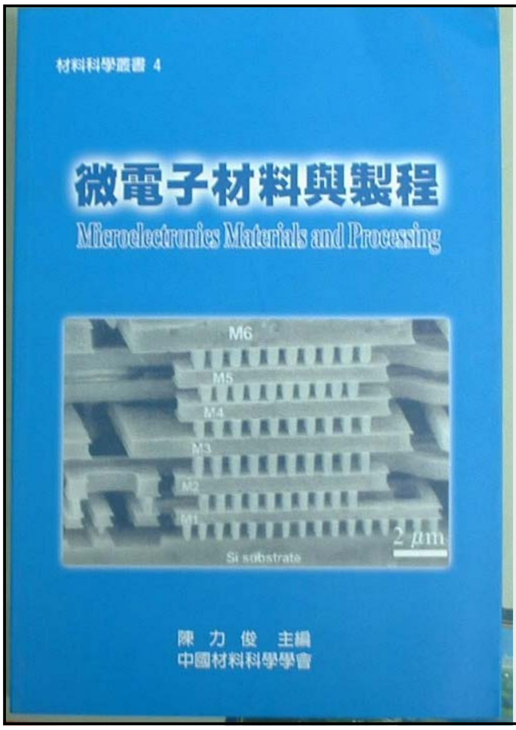
上冊: 群英聚會麻省理工



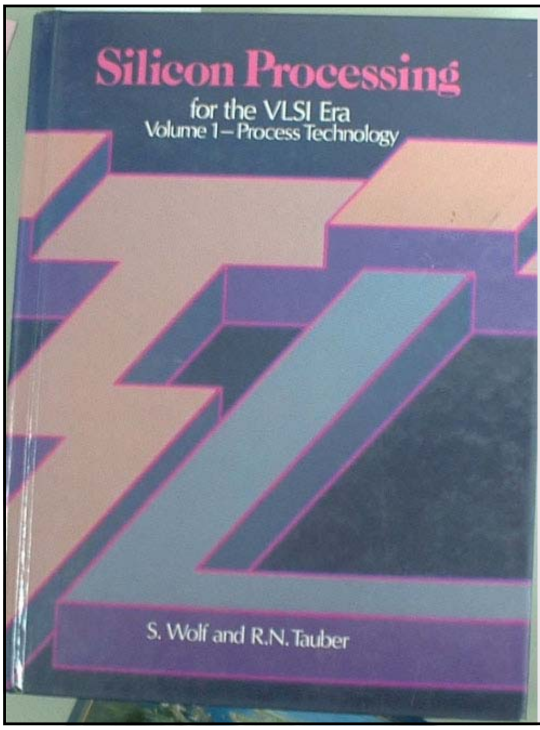
下冊: 輻射八方改造世界



- Plummer et.al, Silicon VLSI Technology



- 陳力俊等
- 微電子材料與製程



- Wolf, Silicon Processing for the VLSI Era

Grading Policy

- Homework 20
  - About 8 -10 times
- 4 Quizzes (選3 if Covid 19 still bothers us!)
  total 70
- Term project 10
- Total = 100
- 作業請準時繳交, 遲交不予計分
- 作業兩次或以上未繳者, 期末成績不予調整

Term Paper

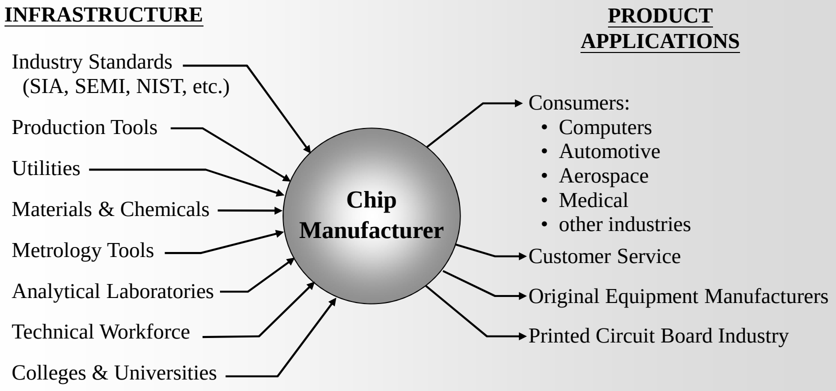
- 過去的 term project 以設計電路製程為目標
  - 同學反應不佳, 不再進行, 改以 term paper
- 出處為IEEE 半導體製造, 微機電設計, 以級封裝相關論文之研讀與報告
- 詳細規定上課時再介紹

Part II: Semiconductor Fabrication 歷史回顧

IC Industries

- Raw material supplier
  - wafers, chemicals
- IC circuitry design
- IC fabrication
  - E.g., TSMC, UMC for fab only
  - E.g., Intel, TI, Lucent for both design and fabrication
- IC fabrication/ characterization equipment supplier
  - CVD system, lithography, CMP
  - E.g., Applied Materials, KLA-Tencor, Nikon

The Semiconductor Industry



INFRASTRUCTURE

- Industry Standards (SIA, SEMI, NIST, etc.)
- Production Tools
- Utilities
- Materials & Chemicals
- Metrology Tools
- Analytical Laboratories
- Technical Workforce
- Colleges & Universities

Chip Manufacturer

PRODUCT APPLICATIONS

- Consumers:
  - Computers
  - Automotive
  - Aerospace
  - Medical
  - other industries
- Customer Service
- Original Equipment Manufacturers
- Printed Circuit Board Industry

Figure 1.1

History of Semiconductor Devices I

- 1890s
  - Mechanical tabulating machine
  - Herman Hollerith
  - Eventually IBM
- 1900s - 1950s
  - Vacuum tubes
- 1930s
  - Electromechanical computers
  - V. Bush at MIT
- 1940s
  - ENIAC, the first electronic computer

History of Semiconductor Devices II

- ENIAC 1947

– size	30 x 50 ft^2
– weight	30 tons
– vacuum tubes	18,000
– resistor	70,000
– capacitor	10,000
– switches	6000
– power	150,000 W
– Cost (1940)	$400,000

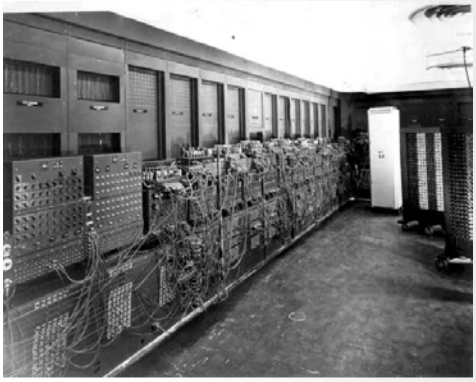
- Same function can be achieved by a 1.5 cm × 1.5 cm die in mid 1970s !

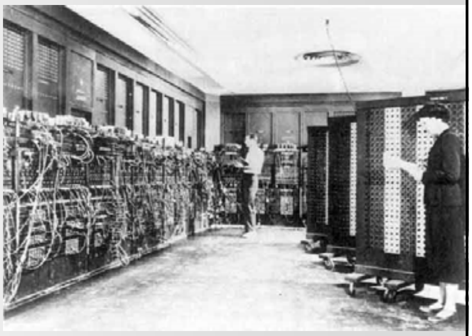
Development of an Industry

- The roots of the electronic industry are based on the vacuum tube and early use of silicon for signal transmission prior to World War II. The first electronic computer, the ENIAC, was developed at the University of Pennsylvania during World War II.

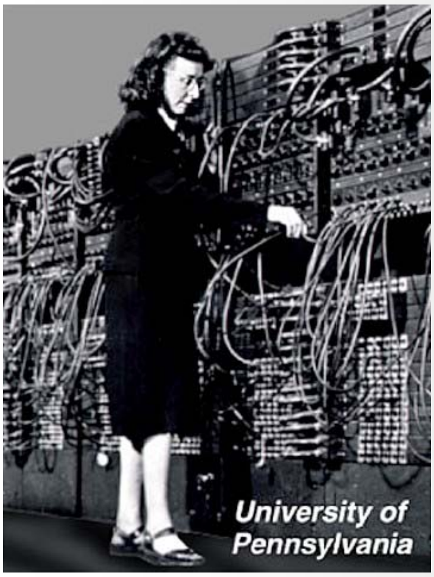
- William Shockley, John Bardeen and Walter Brattain invented the solid-state transistor at Bell Telephone Laboratories on December 16, 1947. The semiconductor industry grew rapidly in the 1950s to commercialize the new transistor technology, with many early pioneers working in Silicon Valley in Northern California.

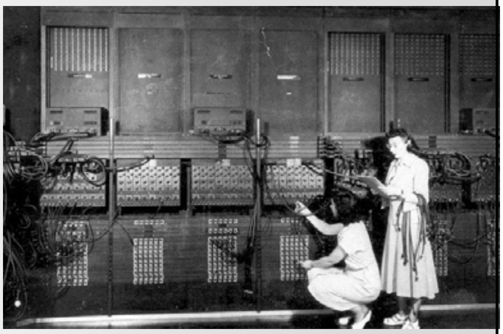
ENIAC





ENIAC





Vacuum Tubes in First Computer

Semiconductor Devices

- Semiconductor is the most important industry in Taiwan
- Related product
  - computer
  - other ICs
  - communication devices
  - MEMS ?
- Can be classified into 3 levels
  - electronics design
  - semiconductor fabrication
  - IC package
- This course is focus on fabrication

History of Semiconductor Devices (III)

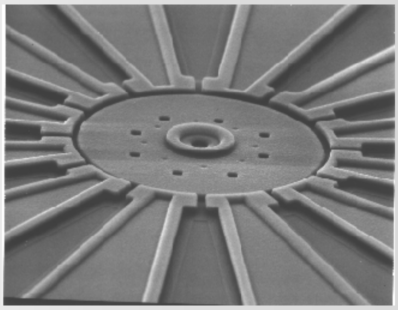
- Dec. 23, 1947
  - The first transfer resistor (Transistor)
  - Bell Laboratory
  - Bardeen, Brattin, Shockley, 1956 Nobel Prize in physics
- First Single Crystal Germanium, 1952
- First Single Crystal Silicon, 1954
- Discrete devices (1950s)
  - one device per chip
  - transistor radios

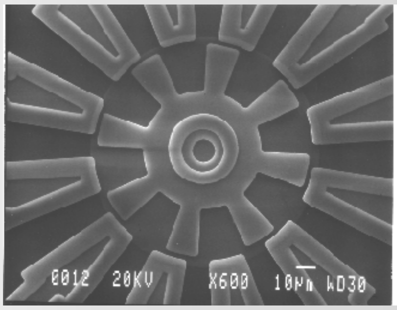
History of Semiconductor Devices (IV)

- Integrated Circuits (ICs)
  - appeared in 1958, J. Kilby, TI (2000 Nobel Physics laureate)
  - 5 devices in the same element
  - wire individual elements in one
- First IC product, Fairchild Camera, 1961
  - Robert Noyce
- First OP AMP
  - ~ 1967
- First CPU
  - ~1971 (4004)

History of Semiconductor Devices (V)

- Microelectromechanical Systems (MEMS)
- 1989 Micro motors
  - UC Berkeley: L-S Fan (now at NTHU), Y-C Tai (now at Caltech)
  - MIT: Meregany (now at Case Western)

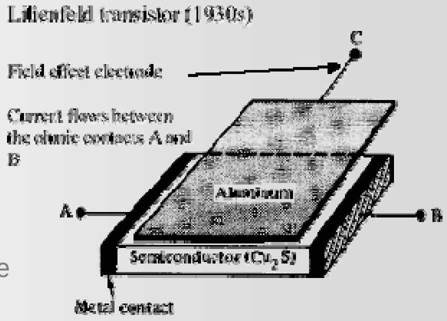




Lilienfeld FET Transistor (1930)

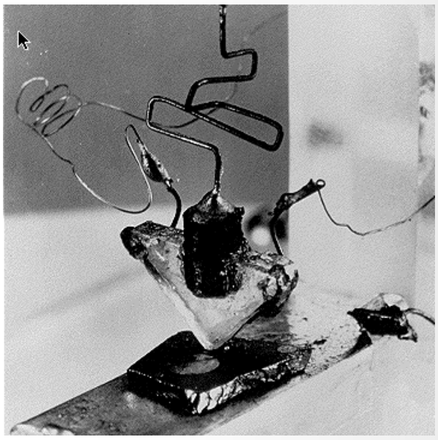
Lilienfeld could not build FET because of excessive surface states at the interface between the oxide and the semiconductor. Charges were so numerous that current flowed with zero bias. It was only possible to turn OFF the device by driving the carriers deep (now called a “depletion mode” FET). Charges were such that only n-type semiconductors could be used. During the 1950s, methods reduced the surface states and enable the fabrication of a normally OFF device with zero bias, “enhancement-mode” FET. The first working MOS-FET was announced in 1960 (ATT).

Now, most MOS-FETs are "enhancement - mode" devices made on p-type silicon.



J. E. Lilienfeld, who obtained several concept patents on a field-effect transistor nearly twenty years before the work on the transistor started at the Bell Telephone Laboratories. The patents created interference with Shockley's application. The photograph is taken from Lilienfeld's U.S. naturalization documents. (Reprinted with permission from *Physics Today* [May 1988]: 87. © 1988 American Institute of Physics.)

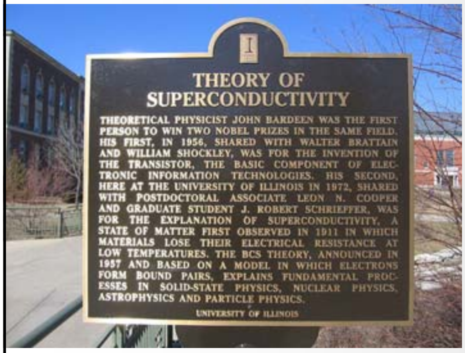
Transistor Age



N	P	N

Dec. 1947

John Bardeen



THEORY OF SUPERCONDUCTIVITY

THEORETICAL PHYSICIST JOHN BARDEEN WAS THE FIRST PERSON TO WIN TWO NOBEL PRIZES IN THE SAME FIELD. HIS FIRST, IN 1956, SHARED WITH WALTER BRATTAIN AND WILLIAM SHOCKLEY, WAS FOR THE INVENTION OF THE TRANSISTOR, THE BASIC COMPONENT OF ELECTRONIC INFORMATION TECHNOLOGIES. HIS SECOND, HERE AT THE UNIVERSITY OF ILLINOIS IN 1972, SHARED WITH POSTDOCTORAL ASSOCIATE LEON N. COOPER AND GRADUATE STUDENT J. ROBERT SCHRIEFFER, WAS FOR THE EXPLANATION OF SUPERCONDUCTIVITY, A STATE OF MATTER FIRST OBSERVED IN 1911 IN WHICH MATERIALS LOSE THEIR ELECTRICAL RESISTANCE AT LOW TEMPERATURES. THE BCS THEORY, ANNOUNCED IN 1957 AND BASED ON A MODEL IN WHICH ELECTRONS FORM BOUND PAIRS, EXPLAINS FUNDAMENTAL PROCESSES IN SOLID-STATE PHYSICS, NUCLEAR PHYSICS, ASTROPHYSICS AND PARTICLE PHYSICS.

UNIVERSITY OF ILLINOIS

Invention of the First Transistor

Bringing it All Together - In the past month, John Bardeen and Walter Brattain had managed to get a large amplification at some frequencies and they'd gotten a small amplification for all frequencies -- now they just had to combine the two. They knew that the key components were a slab of germanium and two gold point contacts just fractions of a millimeter apart. Walter Brattain put a ribbon of gold foil around a plastic triangle, and sliced it through at one of the points. By putting the point of the triangle gently down on the germanium, they saw a fantastic effect -- signal came in through one gold contact and increased as as it raced out the other. The first point-contact transistor had been built (in contrast, Lilienfeld's 1930 FET probably never worked).

Telling the Brass - For a week, the scientists kept their success a secret. William Shockley, the project manager, asked Bardeen and Brattain to show off their little plastic triangle at a group meeting to the lab and the higher-ups on December 23. After the rest of the lab had a chance to look it over and conduct a few tests, it was official -- this tiny bit of germanium, plastic and gold was the first working solid state amplifier.

Brattain attached a single strip of gold foil over the point of a plastic triangle. With a razor blade, he sliced through the gold right at the tip of the triangle. **Two gold contacts just a hair-width apart.** The whole triangle was then held over a crystal of germanium on a spring, so that the contacts lightly touched the surface.

The germanium sat on a metal voltage source. This contraption was the very first semiconductor amplifier, because **when a bit of current came through one of the gold contacts, another even stronger current came out the other contact**.

Here's how it worked: The germanium had an excess of electrons, but when an electric signal traveled in through the gold foil, it injected holes (the opposite of electrons) into the surface. This created a thin layer along the top of the germanium with too few electrons. Semiconductors with too many electrons are known as N-type and semiconductors with too few electrons are known as P-type. The boundary between these two kinds of semiconductors is known as a P-N Junction. In the case of Brattain's transistor, current flowed from the base towards the second gold contact. **A small current in one contact controls a larger separate current out the second contact. A little current can alter the flow of a much bigger one, effectively amplifying it.**

The First Transistor Product

Sony

The first transistor radio was a joint project of the Regency Co. and Texas Instruments. TI built the transistors; Regency built the radio. On October 18, 1954, the Regency TR1 was put on the market. It was a scant five inches high and used four germanium transistors. It was discontinued in 1955.

In Japan, a tiny company had other ideas. **Tsushin Kogyo** was close to manufacturing its first radios when it heard that an American company had beaten them to market. But they persevered and made a radio, the TR-52. When Regency quit producing their radio, the Japanese company immediately started shipping their radio to the U.S. One immediate problem was that Americans couldn’t pronounce their name. The founders, Ibuka and Morita, thought of using a Latin word **sonus** meaning "*sound.*" Akio Morita knew some English, and made a simple variation that became their name from then on: SONY

1956 -William Shockley had gone as far as he was going to go at Bell Labs. His patent for an FET had been disallowed when Lilienfeld’s early patents were discovered. He watched the people underneath him get promoted above him -- and with good reason. Too many top quality scientists hadn't been able to work with him . A genius he may have been, but a good manager he was not.

Shockley was lured to the Palo Alto area by Stanford's provost, Fred Terman who thought that a solid research institution in the area would benefit Stanford. With a location picked out, Shockley just had to find the best people. He first sought to employ his colleagues from Bell Labs, but they wouldn't make the jump to the west coast -- or perhaps they couldn't make the jump to working with Shockley again. So Shockley began traveling all over the country recruiting young scientists. of 1956, Shockley and Beckman announced the formation of their brand new lab. They only had four employees at the time, but ***Shockley Semiconductor Laboratory*** had officially opened for business.

In May of 1957, just over a year after the company was founded, eight employees went to CEO Arnold Beckman and explained that they couldn't work with Shockley as their manager anymore. One problem was the enforced polygraph testing of employees to “prove their loyalty”. The "traitorous eight“ resigned. The next day they signed a contract for $1.3 million with a New York firm called **Fairchild Camera and Instruments** which was involved with missiles and satellite systems. The eight men were Julius Blank, Victor Grinich, Jean Hoerni, Gene Kleiner, Jay Last, **Gordon Moore, Robert Noyce**, and Sheldon Roberts.

Three years later Moore and Noyce left to found **Intel**.

Circuits Integration

- The first integrated circuit, or IC, was independently co-invented by Jack Kilby at Texas Instruments and Robert Noyce at Fairchild Semiconductor in 1959. An IC integrates multiple electronic components on one substrate of silicon.
- Circuit integration eras are: small scale integration (SSI) with 2 - 50 components, medium scale integration (MSI) with 50 – 5k components, large scale integration (LSI) with 5k to 100k components, very large scale integration (VLSI) with 100k to 1M components, and ultra large scale integration (ULSI) with > 1M components.

Invention of the Integrated Circuit

In 1952, Dummer said: "It is possible to envision electronic equipment in a solid block with no connecting wires. The block may consist of layers of insulating, conducting, rectifying and amplifying materials, the electrical functions being connected directly by cutting out areas of the various layers"

In July, 1958, **Jack Kilby** was sitting alone at Texas Instruments. He had been hired only a couple of months earlier and the halls were deserted. It occurred to him that all parts of a circuit, not just the transistor, could be made out of silicon. By September 12, Kilby had built a working model, and on February 6, Texas Instruments filed a patent. Their first "Solid Circuit" the size of a pencil point, was shown off for the first time in March.

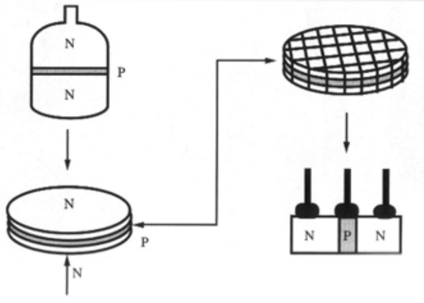
In California, another man had similar ideas in January, 1959. Robert Noyce was working at the small Fairchild Semiconductor startup company. He also realized a whole circuit could be made on a single chip. While Kilby had hammered out the details of making individual components, Noyce thought of a much better way to connect the parts. That spring, Fairchild began a push to build what they called "unitary circuits" and they also applied for a patent on the idea. Knowing that TI had already filed a patent on something similar, Fairchild wrote out a highly detailed application, hoping that it wouldn't infringe on TI 's similar device.

All that detail paid off. In April, 1961, the patent office awarded the first patent for an integrated circuit to Robert Noyce while Kilby's application was still being analyzed. Today, both men are acknowledged as having independently conceived of the idea.

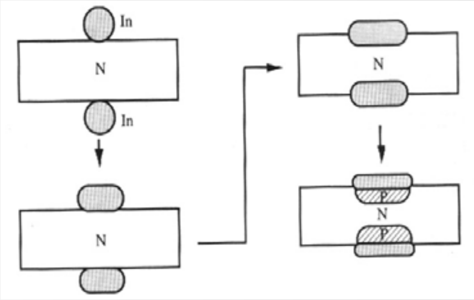
The “Invention” of the Integrated Circuit

- Jack Kilby of Texas Instruments filed a Patent Application for an integrated circuit in the summer of 1958. It was an phase–shift oscillator circuit on a germanium substrate which used external wires between components. Edward Noyce of Fairchild Semiconductor (co-founder of Intel) filed a Patent Application for an integrated circuit in Jan, 1959, focussed on silicon substrates with thin film Al interconnects. Noyce received his silicon patent a year before Kilby received a more general patent. Since the Noyce patent centered on silicon substrates and planar interconnections (etched Al), it was equally valuable as the broader Kilby patent.
- Both companies patented and marketed their integrated circuits. A drawn-out court battle between TI and Fairchild over integrated circuit patents consumed the best part of a decade. Finally, a settlement was reached in 1969, whereby both Kilby and Noyce recognized each other as equal co-inventors of the integrated circuit.
- Kilby was awarded the Nobel Prize in 2000 for his Integrated Circuit work. Ed Noyce died in 1990, and hence was ineligible for the Prize (given only to living persons).

Process Development



Grown junction transistor technology



Alloy junction technology

The First Planar Transistor

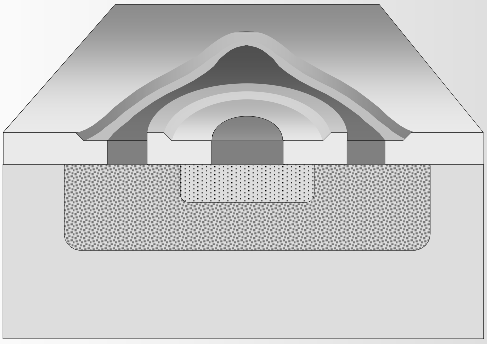
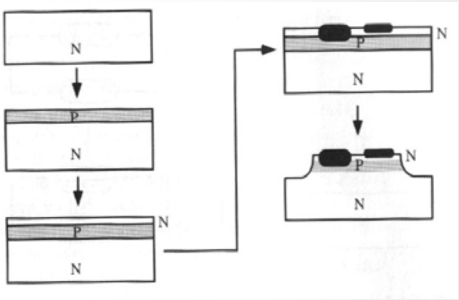
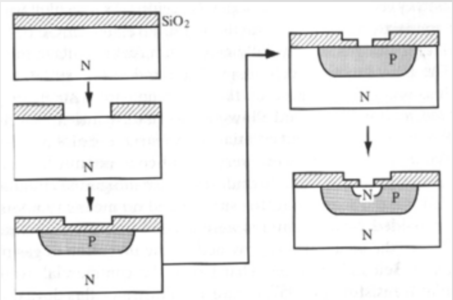


Figure 1.2

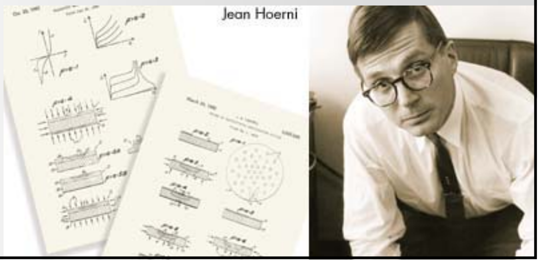
Process Development





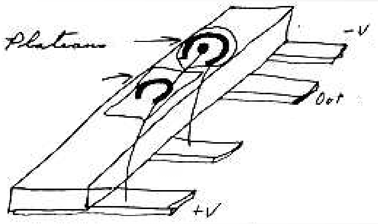
Double diffused mesa
transistor technology

Planar process, 1958



Jean Hoerni, inventor
of planar process

First IC Device Made by Jack Kilby of Texas Instrument in 1958



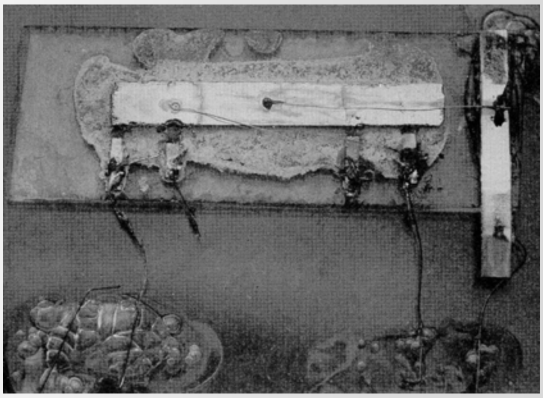
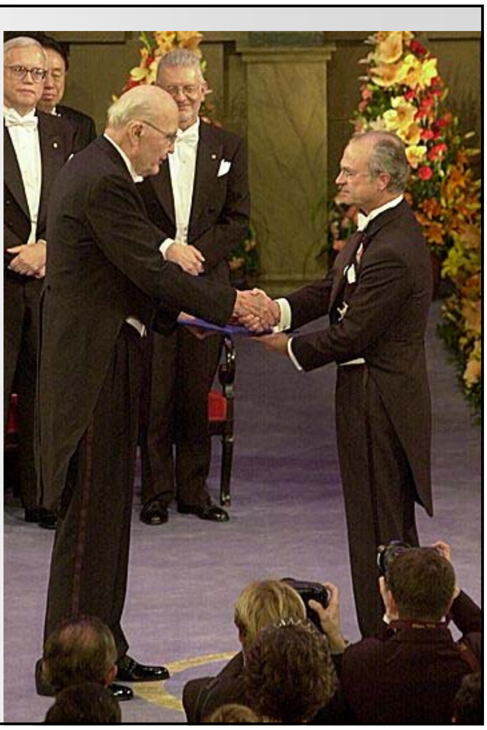


Photo courtesy: Texas Instruments

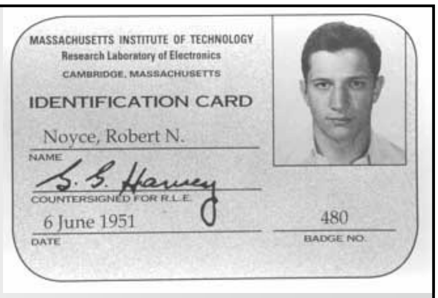
Jack Kilby



- 1958

Intel

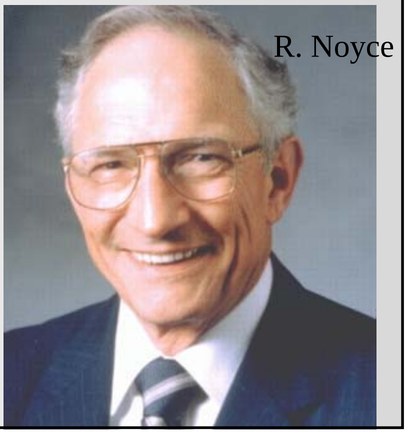
D. Moore



MASSACHUSETTS INSTITUTE OF TECHNOLOGY
Research Laboratory of Electronics
CAMBRIDGE, MASSACHUSETTS

IDENTIFICATION CARD

Noyce, Robert N.
NAME
S. G. Harvey
COUNTERSIGNED FOR R.L.E.
6 June 1951
DATE
480
BADGE NO.



R. Noyce

4001

First Silicon IC Chip Made by Robert Noyce of Fairchild Camera in 1961

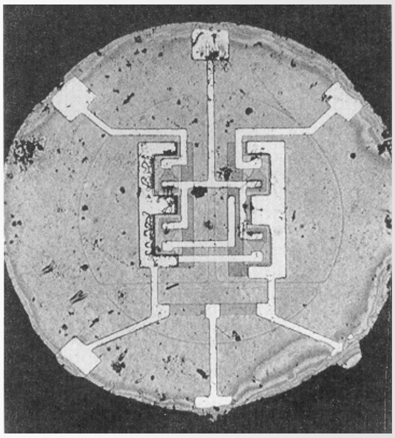
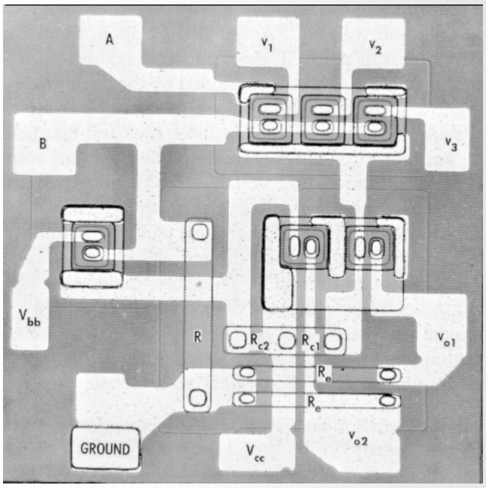


Photo courtesy: Fairchild Semiconductor International

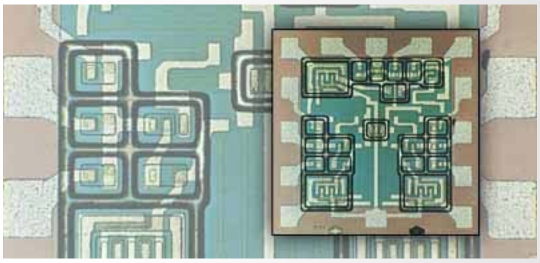
Early Integrated Circuits



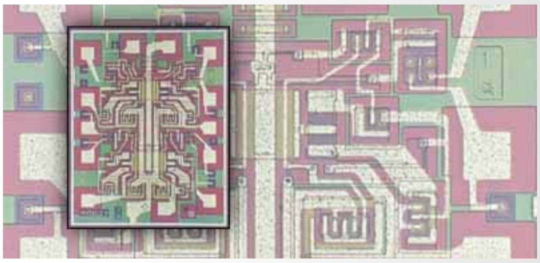
Bipolar logic
1960's

ECL 3-input Gate/SRAM
Motorola 1966

OPAMP & TTL Logic Circuit

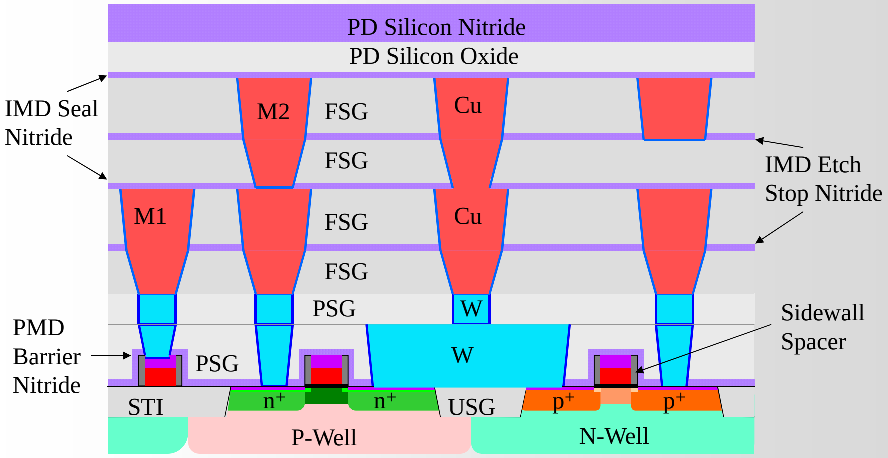


The 1st OPAMP

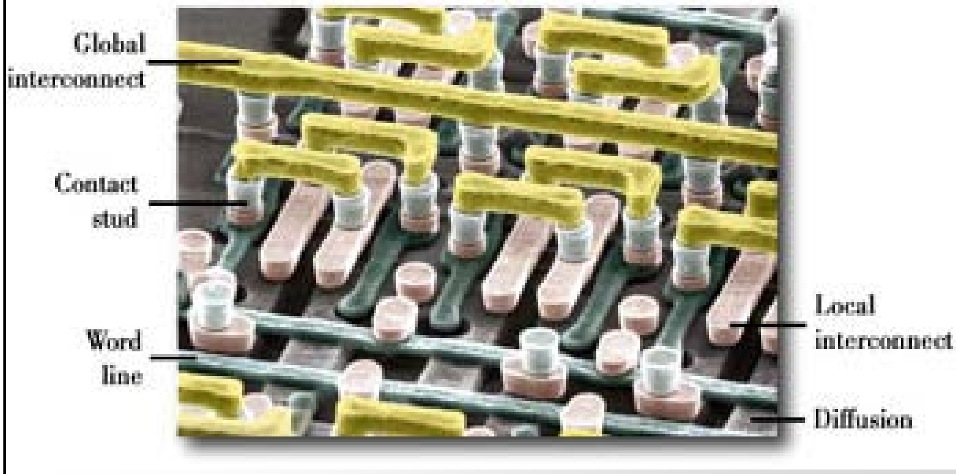


The 1st TTL logic IC

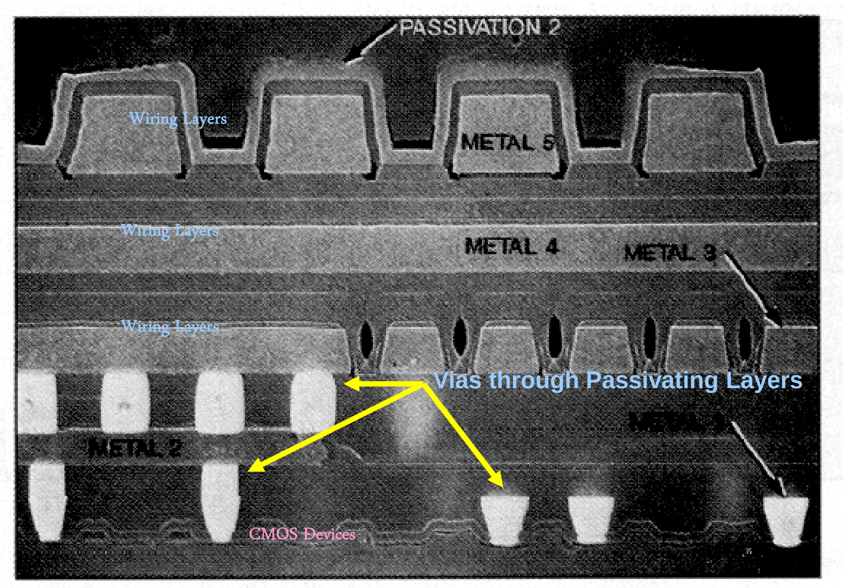
Cross-Section of Typical Modern CMOS Elements



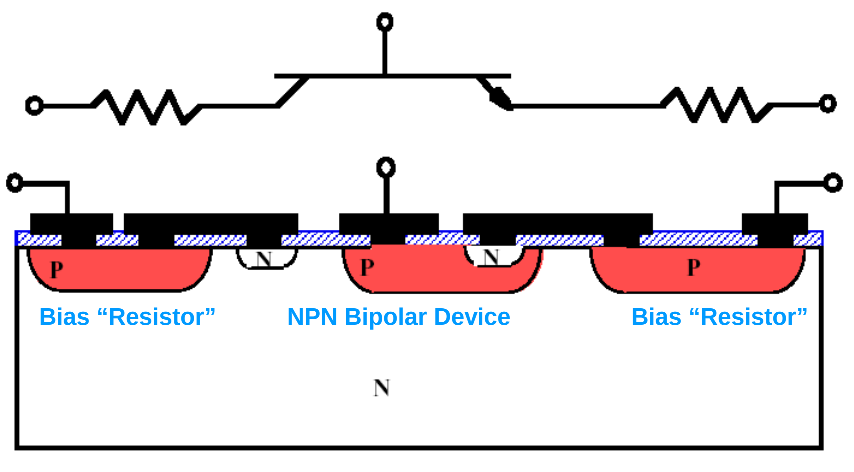
Interconnections



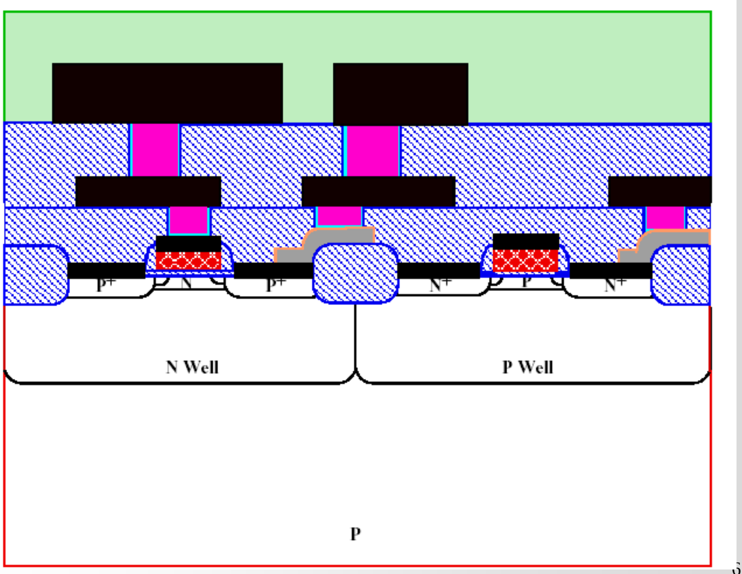
SEM Cross-Section of Integrated Circuit



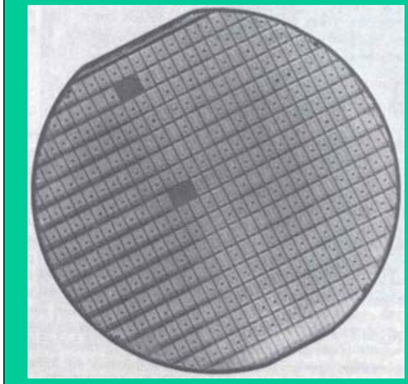
Basic Bipolar Paired Transistors

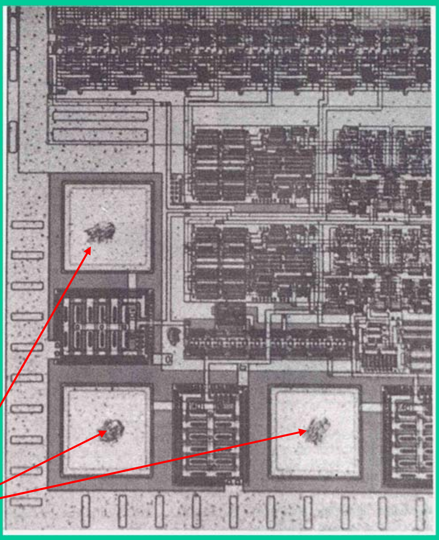


Modern Integrated Circuit Section



Wafer with IC Chips



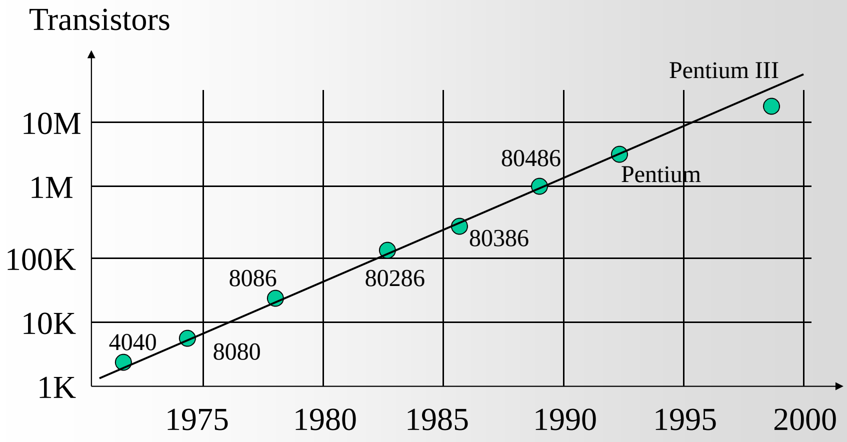


Thin film pads for wire bonding

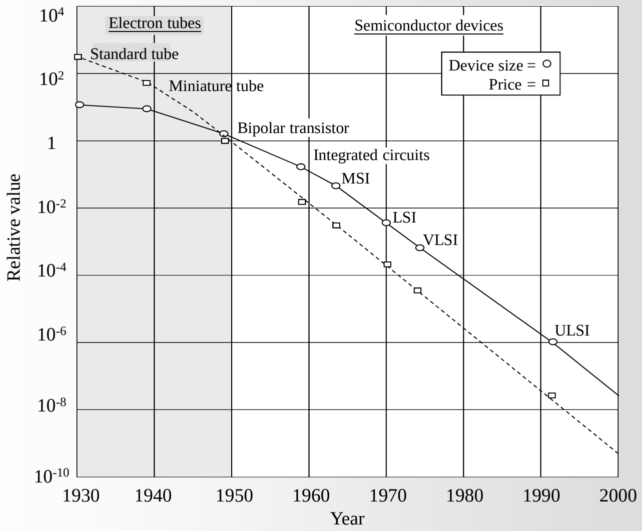
Moore’s Law

- Intel co-founder Gorden Moore notice in 1964
- Number of transistors doubled every 12 months while price unchanged
- Slowed down in the 1980s to every 18 months
- Amazingly still correct, likely to keep until 2010.

Moore’s Law, Intel’s Version



Price Decrease of Semiconductor Chips

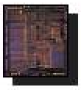
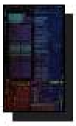
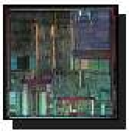


Redrawn from C. Chang & S. Sze, McGraw-Hill, *ULSI Technology*, (New York: McGraw-Hill, 1996), xxiii. Figure 1.15

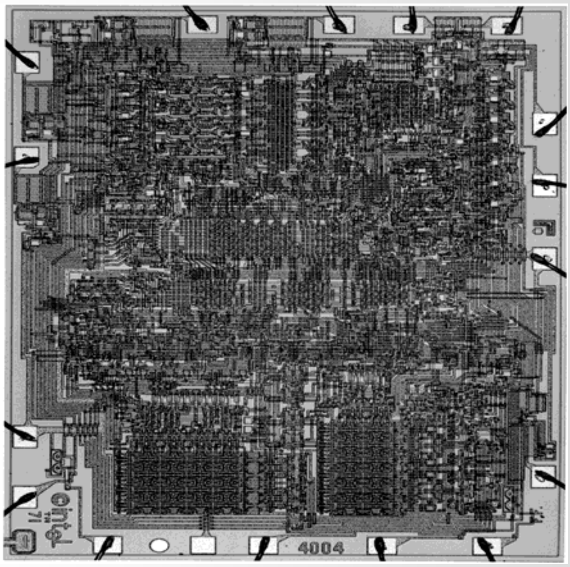
The Power of Moore’s Law

- ENIAC 1947
  - size 30 x 50 ft^2
  - weight 30 tons
  - vacuum tubes 18,000
  - resistor 70,000
  - capacitor 10,000
  - switches 6000
  - power 150,000 W
  - Cost (1940) $400,000
- Same function can be achieved by a 1.5 cm × 1.5 cm die in mid 1970s !

The Effect of Size

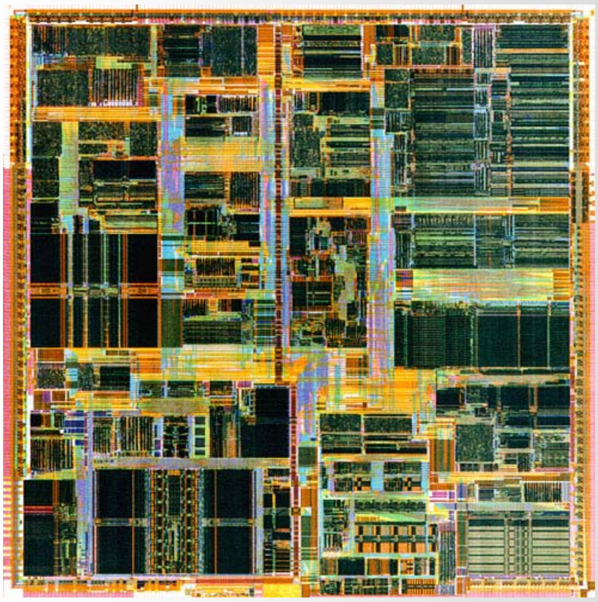
Generation:	**1.5µ**	**1.0µ**	**0.8µ**	**0.6µ**	**0.35µ**	**0.25µ**
Intel386™ DX Processor						
Intel486™ DX Processor						
Pentium® Processor						
Pentium® II Processor						

Intel 4004 Microprocessor



1971
1 MHz, 5V
5k Components

Intel Pentium (III) Microprocessor

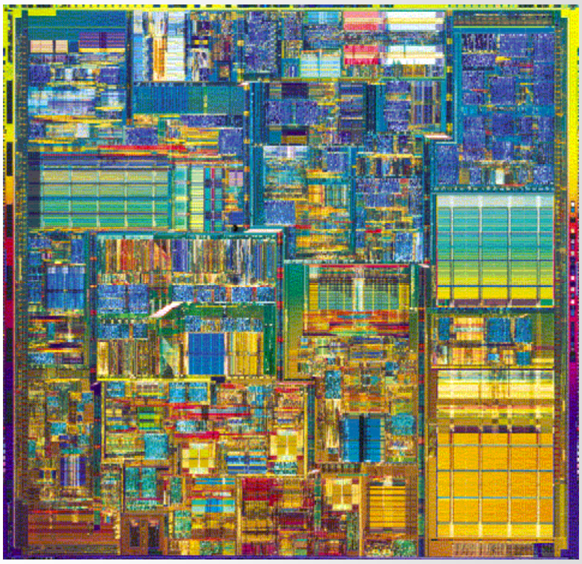


1994

100 MHz, 3.3V

3M Components

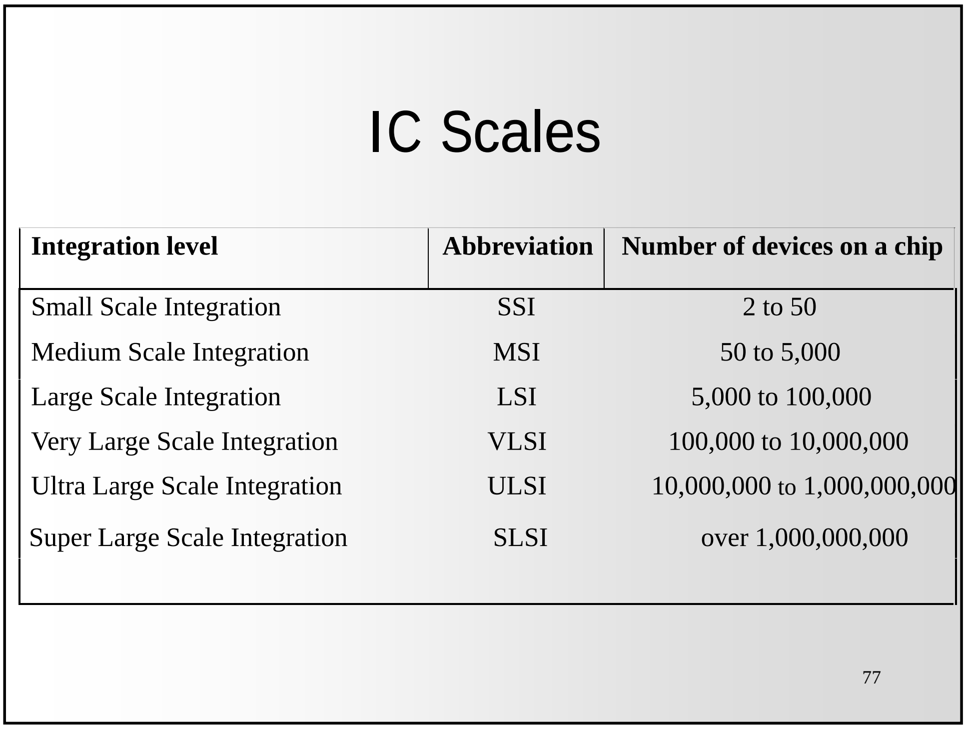
Intel Pentium (IV) Microprocessor



1999

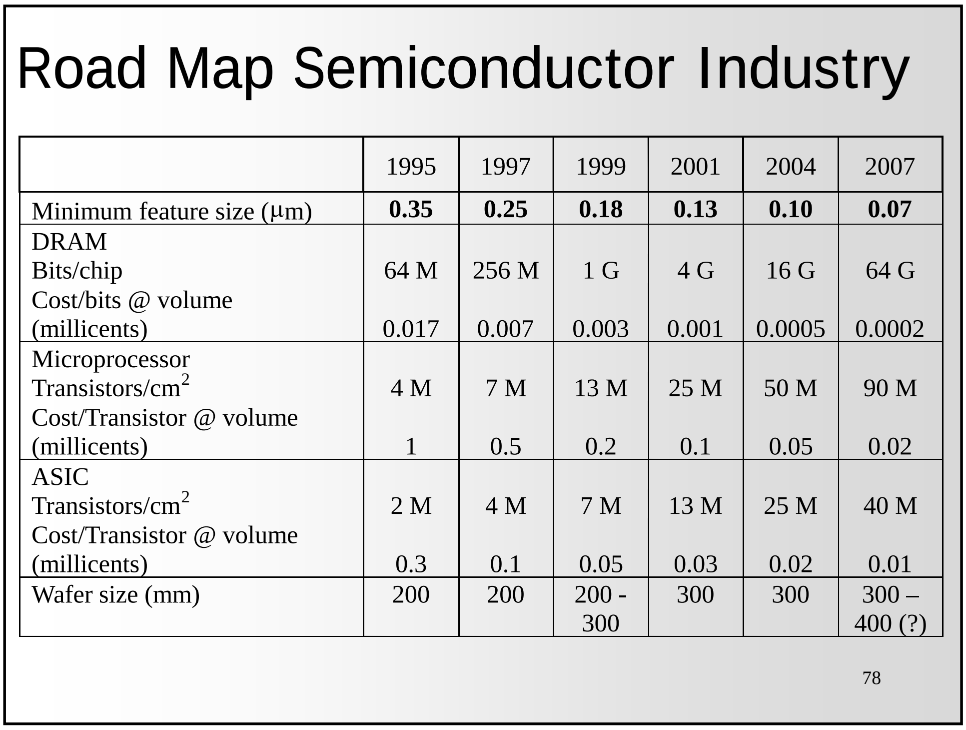
1.2 GHz, 1.8V

42M Components



IC Scales

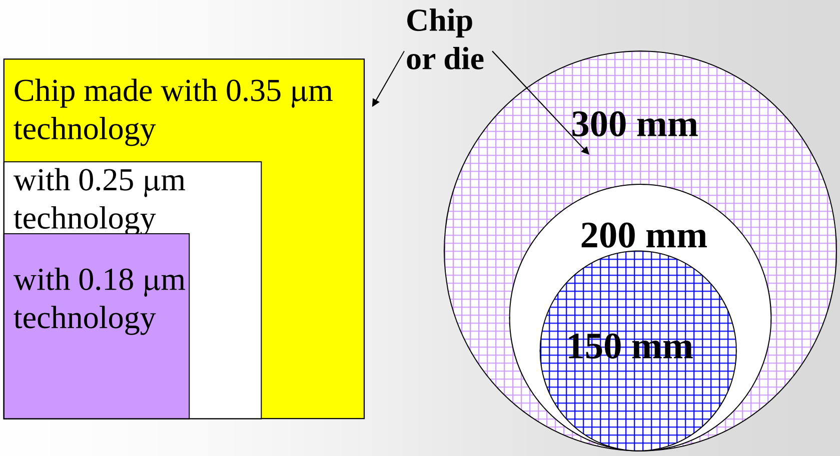
Integration level	**Abbreviation**	**Number of devices on a chip**
Small Scale Integration	SSI	2 to 50
Medium Scale Integration	MSI	50 to 5,000
Large Scale Integration	LSI	5,000 to 100,000
Very Large Scale Integration	VLSI	100,000 to 10,000,000
Ultra Large Scale Integration	ULSI	10,000,000 to 1,000,000,000
Super Large Scale Integration	SLSI	over 1,000,000,000



Road Map Semiconductor Industry

	1995	1997	1999	2001	2004	2007
Minimum feature size (μm)	**0.35**	**0.25**	**0.18**	**0.13**	**0.10**	**0.07**
DRAM						
Bits/chip	64 M	256 M	1 G	4 G	16 G	64 G
Cost/bits @ volume (millicents)	0.017	0.007	0.003	0.001	0.0005	0.0002
Microprocessor						
Transistors/cm^2	4 M	7 M	13 M	25 M	50 M	90 M
Cost/Transistor @ volume (millicents)	1	0.5	0.2	0.1	0.05	0.02
ASIC						
Transistors/cm^2	2 M	4 M	7 M	13 M	25 M	40 M
Cost/Transistor @ volume (millicents)	0.3	0.1	0.05	0.03	0.02	0.01
Wafer size (mm)	200	200	200 - 300	300	300	300 – 400 (?)

Feature Size and Wafer Size



Chip made with 0.35 μm technology

with 0.25 μm technology

with 0.18 μm technology

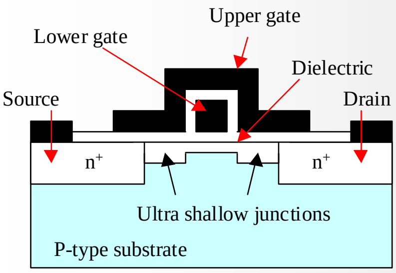
Chip or die

300 mm

200 mm

150 mm

Smallest Known Transistor Made by NEC in 1997



0.014 micron lower gate width

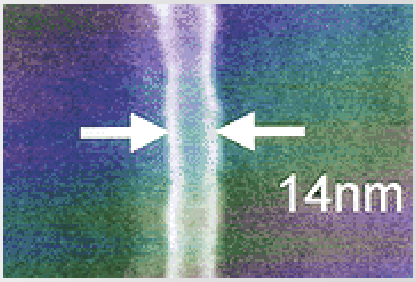


Photo courtesy: NEC Corporation

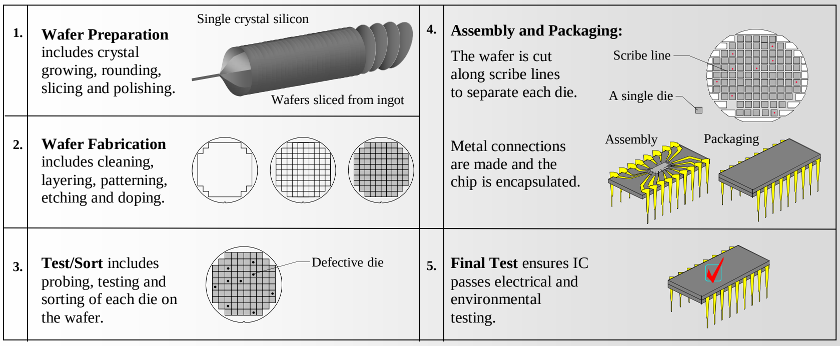
Now the technology is pushing on 2 nm

Limit of the IC device

- Atom size: several Å
- Need some atoms to form a device
- Likely the final limit is around 100 Å or 0.01 micron.
- About 30 silicon atoms

Part III. IC Fabrication Overview

Stages of IC Fabrication



1\. **Wafer Preparation** includes crystal growing, rounding, slicing and polishing.

2\. **Wafer Fabrication** includes cleaning, layering, patterning, etching and doping.

3\. **Test/Sort** includes probing, testing and sorting of each die on the wafer.

4\. **Assembly and Packaging:**

The wafer is cut along scribe lines to separate each die.

Metal connections are made and the chip is encapsulated.

5\. **Final Test** ensures IC passes electrical and environmental testing.

IC Fabrication

- Chips (or die) are fabricated on a thin slice of silicon, known as a wafer (or substrate). Wafers are fabricated in a facility known as a wafer fab, or simply fab.

- The five stages of IC fabrication are:
  - Wafer preparation: silicon is purified and prepared into wafers.
  - Wafer fabrication: microchips are fabricated in a wafer fab by either a merchant chip supplier, captive chip producer, fabless company or foundry.
  - Wafer test: Each individual die is probed and electrically tested to sort for good or bad chips.
  - Assembly and packaging: Each individual die is assembled into its electronic package.
  - Final test: Each packaged IC undergoes final electrical test.

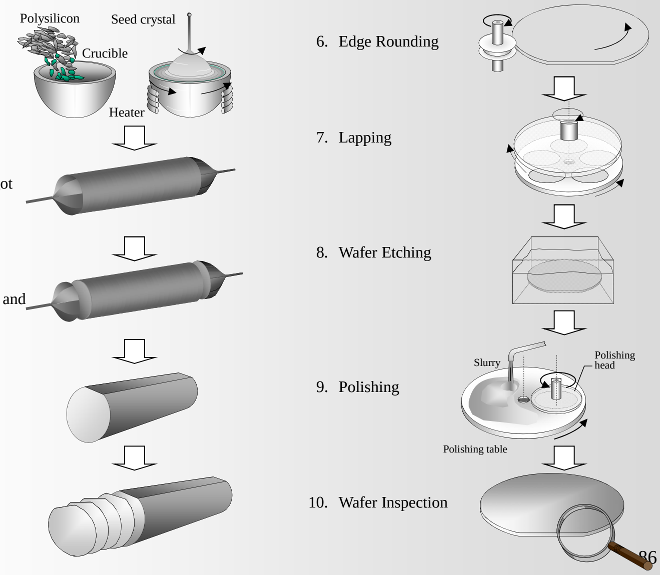
Key Semiconductor Trends

- Increase in chip performance through reduced critical dimensions (CD), more components per chip (Moore’s law, which predicts the doubling of components every 18-24 months) and reduced power consumption.

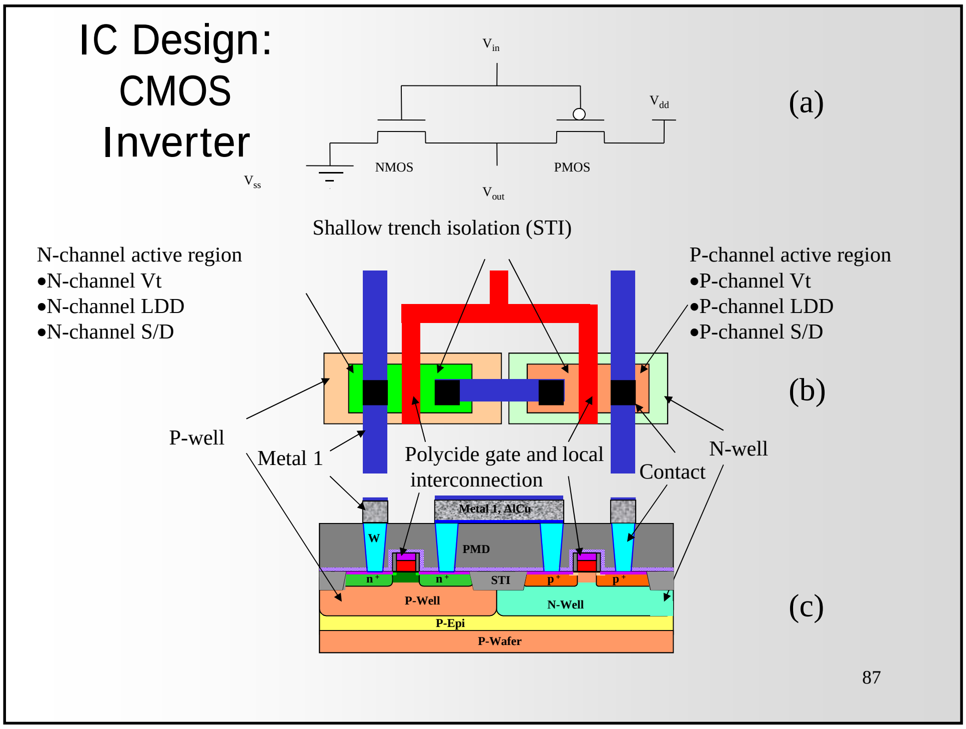
- Increase in chip reliability during usage.

- Reduction in chip price, with an estimated price reduction of 100 million times for the 50 years prior to 1996.

Preparation of Silicon Wafers



1. Crystal Growth
2. Single Crystal Ingot
3. Crystal Trimming and Diameter Grind
4. Flat Grinding
5. Wafer Slicing
6. Edge Rounding
7. Lapping
8. Wafer Etching
9. Polishing
10. Wafer Inspection

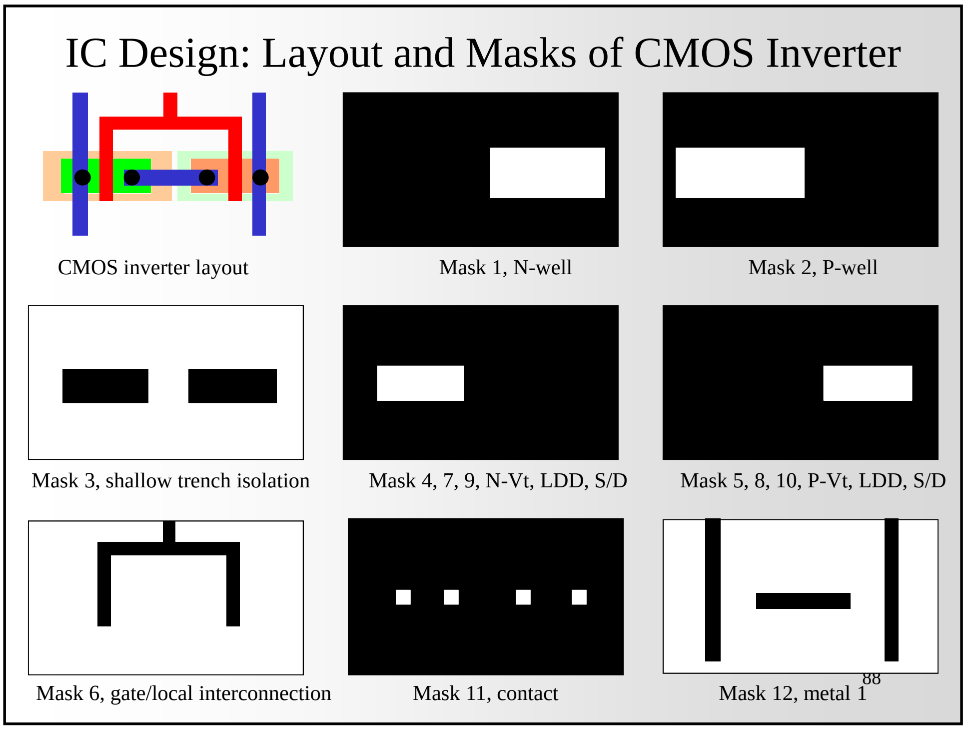


IC Design: CMOS Inverter

Shallow trench isolation (STI)

N-channel active region
- N-channel Vt
- N-channel LDD
- N-channel S/D

P-channel active region
- P-channel Vt
- P-channel LDD
- P-channel S/D



IC Design: Layout and Masks of CMOS Inverter

CMOS inverter layout

Mask 1, N-well

Mask 2, P-well

Mask 3, shallow trench isolation

Mask 4, 7, 9, N-Vt, LDD, S/D

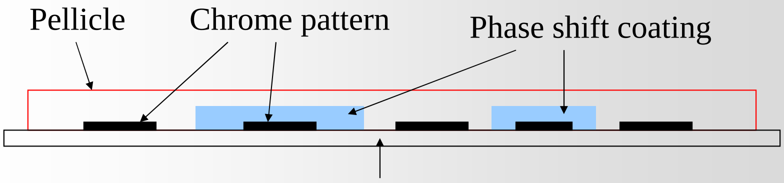
Mask 5, 8, 10, P-Vt, LDD, S/D

Mask 6, gate/local interconnection

Mask 11, contact

Mask 12, metal 1

Mask/Reticle



A Mask and a Reticle

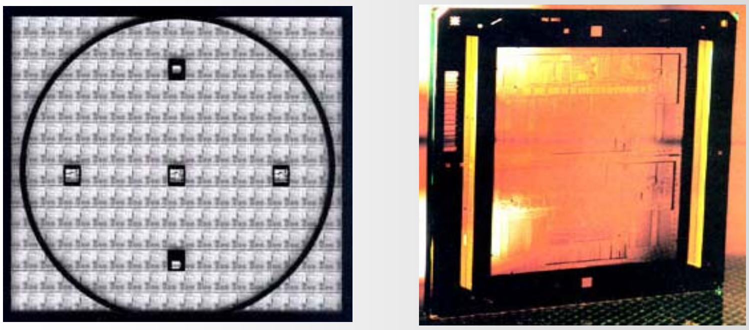
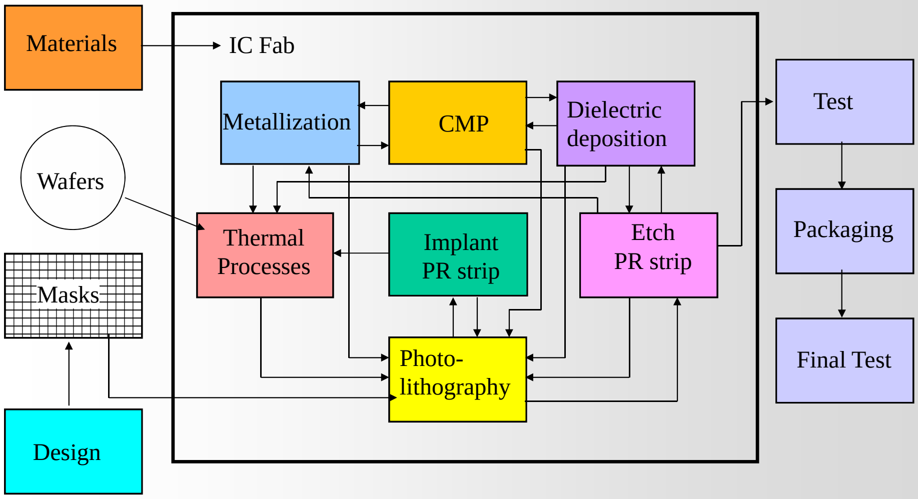


Photo courtesy: SGS Thompson

Wafer Process Flow



Materials

Wafers

Masks

Design

IC Fab

Metallization

CMP

Dielectric deposition

Thermal Processes

Implant PR strip

Etch PR strip

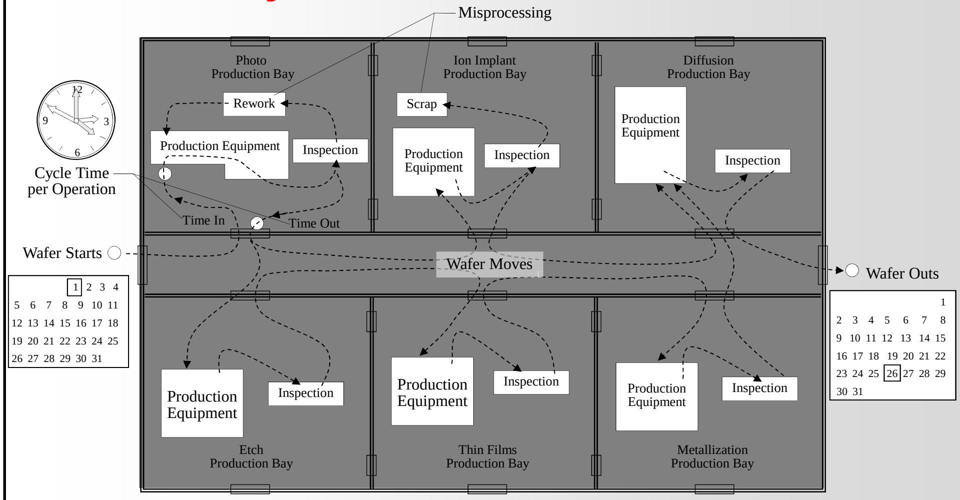
Photo-lithography

Test

Packaging

Final Test

Productivity Measurements in a Wafer Fab



Misprocessing

Cycle Time per Operation

Wafer Starts

Wafer Outs

Wafer Moves

Photo Production Bay

Rework

Production Equipment

Inspection

Time In

Time Out

Ion Implant Production Bay

Scrap

Production Equipment

Inspection

Diffusion Production Bay

Production Equipment

Inspection

Etch Production Bay

Production Equipment

Inspection

Thin Films Production Bay

Production Equipment

Inspection

Metallization Production Bay

Production Equipment

Inspection

Production Cycle Time = (Date and Time of Wafer Start) - (Date and Time of Wafer Out)

Wafer Outs = Wafer Starts - Wafers Scrapped

Operator Efficiency = Theoretical Cycle Time / Actual Cycle Time

范揚楷部經理
機械系 1990級
TSMC F14B

Prof. Arturo
Ayon
U. Texas

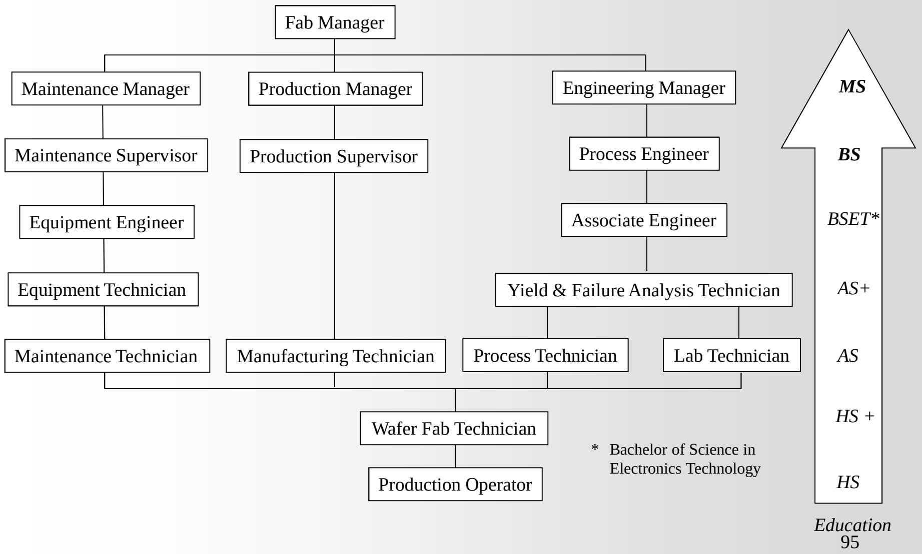
Prof. Kevin Turner
U. Pennsylvania

江浩寧博士
TSMC 主任工
程師

Equipment Technician in a Wafer Fab

Photograph courtesy of Advanced Micro Devices

Career Paths in the Semiconductor Industry


Fab Manager

Maintenance Manager
Maintenance Supervisor
Equipment Engineer
Equipment Technician
Maintenance Technician

Production Manager
Production Supervisor
Manufacturing Technician

Engineering Manager
Process Engineer
Associate Engineer
Yield & Failure Analysis Technician
Process Technician
Lab Technician

Wafer Fab Technician
Production Operator

MS
BS
*BSET**
AS+
AS
HS +
HS

Education

* Bachelor of Science in Electronics Technology

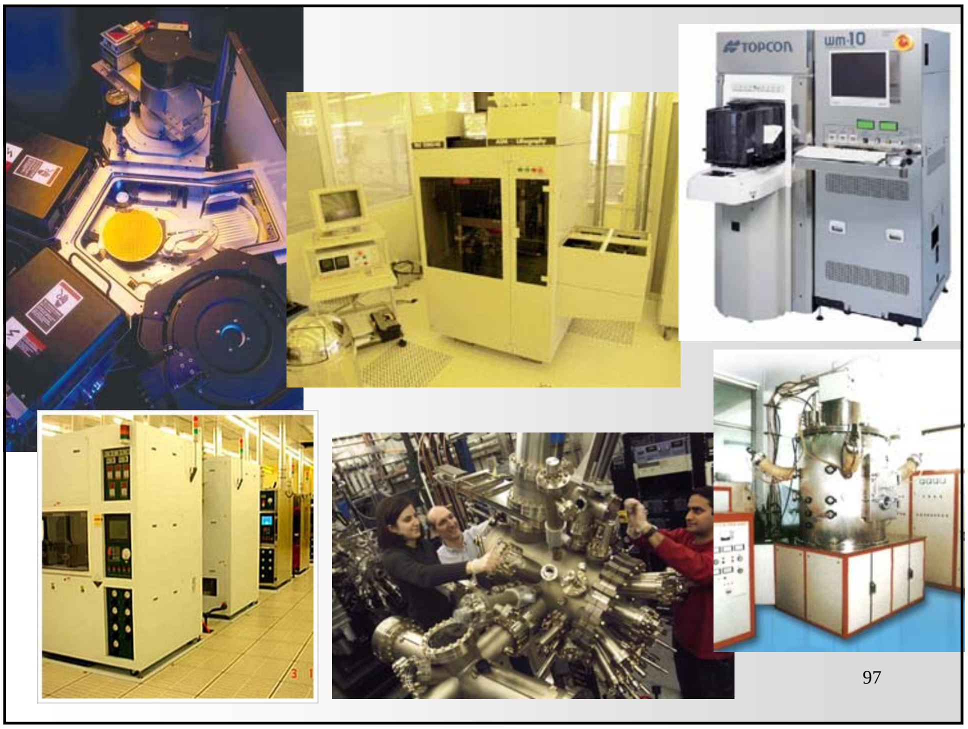
Semiconductor Equipment Suppliers

Applied Materials, founded in 1967 by McNeilly and Benzing

ASML, found in 1984

KLA-Tencor, 1997

HMI 1998



江湖武術比喻 (From: 法櫃奇兵 1980)

Gun >> Knife (製程設備性能的重要性)
Equipment dominates Performance !!!

晶圓代工

UMC
聯 華 電 子

intel

tsmc
台灣積體電路製造股份有限公司
Taiwan Semiconductor Manufacturing Company, Ltd.

SAMSUNG

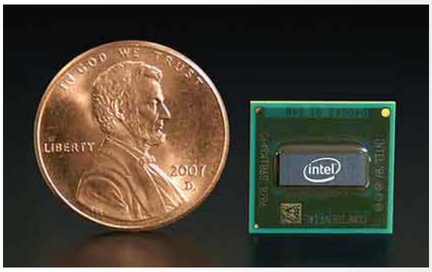
GLOBAL
FOUNDRIES

Wafer Fab

Photo courtesy of Advanced Micro Devices-Dresden, © S. Doering

Photo 1.6

TSMC Fab 14



Intel Atom CPU

Packaging

ASE GROUP
日月光集團

南茂科技股份有限公司
ChipMOS TECHNOLOGIES INC.

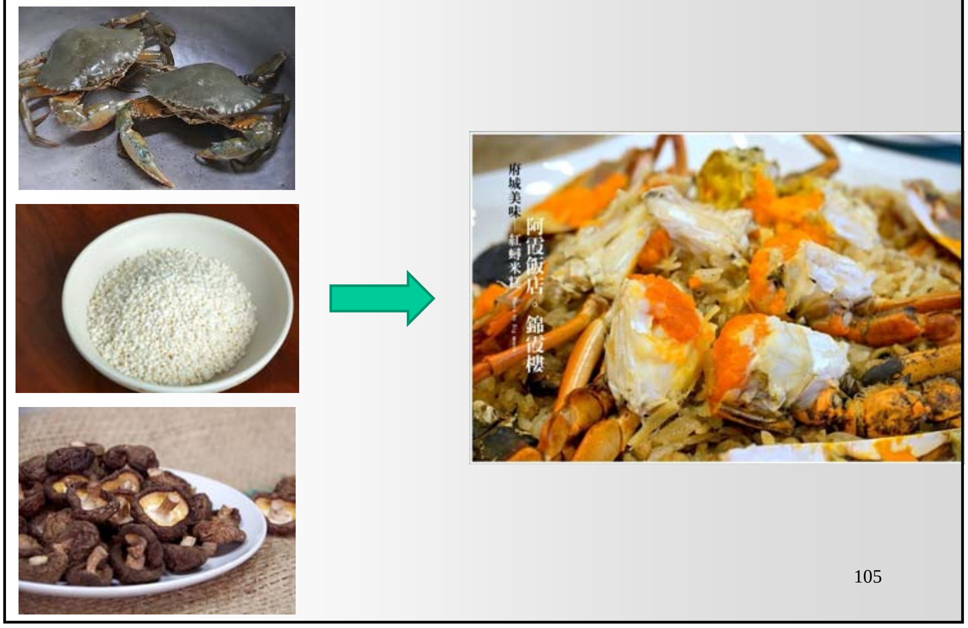
A Comment

- 一般人會認為, (晶圓代工廠) 為什麼要把員工操那麼累, 少賺一點又如何?
- Real Situation
  - 越來越接近贏者全拿, 輸的連分一杯羹的機會都沒有.
    - 打擊率 2.5成, 年薪50萬美金. 打擊率 3成, 年薪2500萬美金.
  - 勝負間的差異不大, 不刻意努力, 一兩年後便會被超越....然後 ....

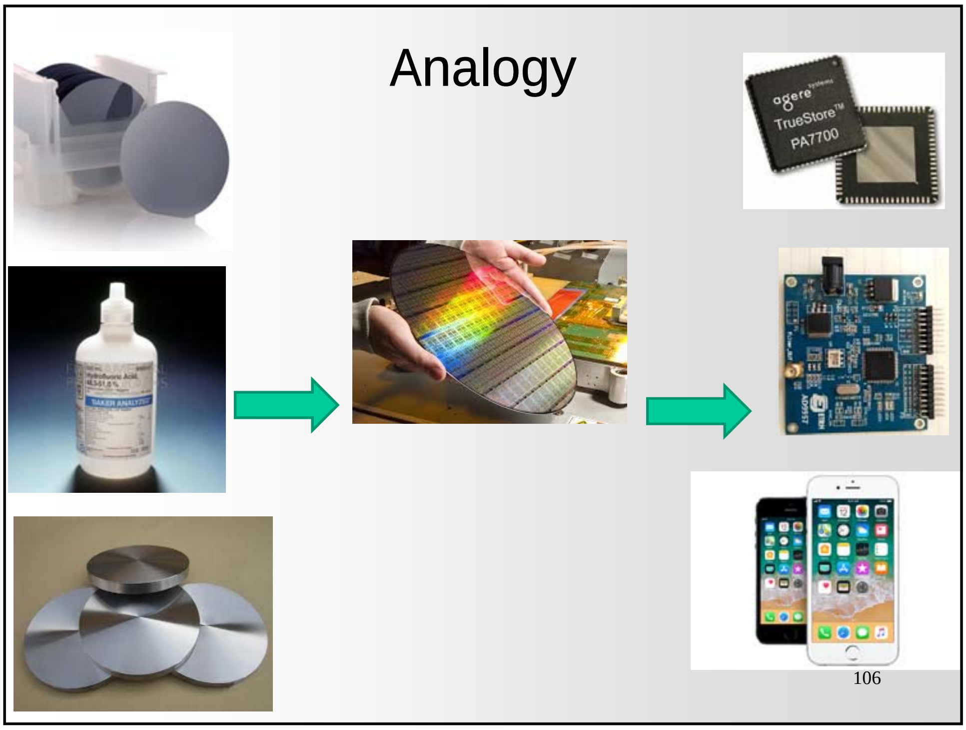
  - 因此, 操得那麼累, 與其說是賺大錢, 倒不如說是求生存.
  - 當然, 若能生存下來, 擊敗對手, 收益當然沒問題.

Part IV: Individual Process Overview

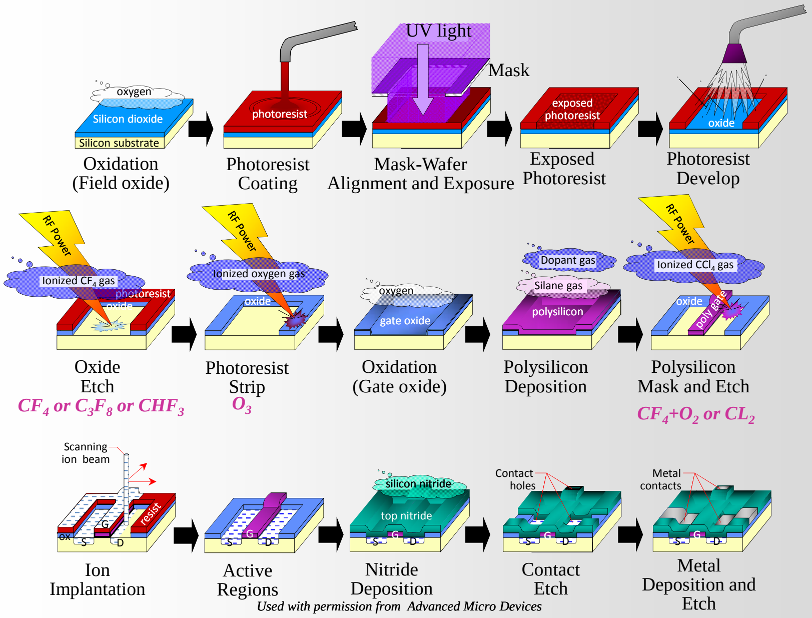
Analogy



Analogy



Major Fabrication Steps in MOS Process Flow



Used with permission from Advanced Micro Devices

Figure 9.1

CMOS Process Flow

- Overview of Areas in a Wafer Fab
  - Diffusion
  - Photolithography
  - Etch
  - Ion Implant
  - Thin Films
  - Polish
- CMOS Manufacturing Steps
- Parametric Testing

Diffusion & Oxidation

Oxide Layer Dopant Barrier

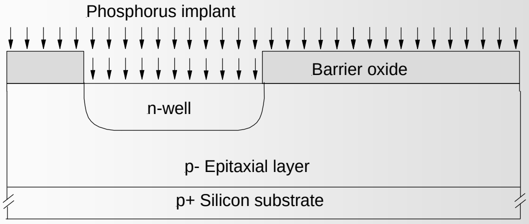


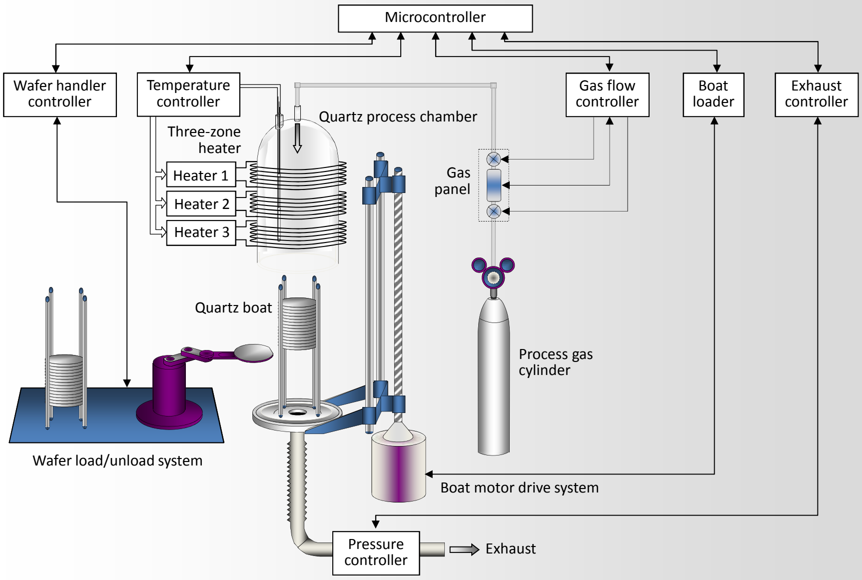
Figure 10.5

Vertical Diffusion Furnace

Photograph courtesy of International SEMATECH

Photo 10.2

Block Diagram of Vertical Furnace System



Microcontroller

Wafer handler controller

Temperature controller

Gas flow controller

Boat loader

Exhaust controller

Quartz process chamber

Three-zone heater

Heater 1

Heater 2

Heater 3

Gas panel

Quartz boat

Process gas cylinder

Wafer load/unload system

Boat motor drive system

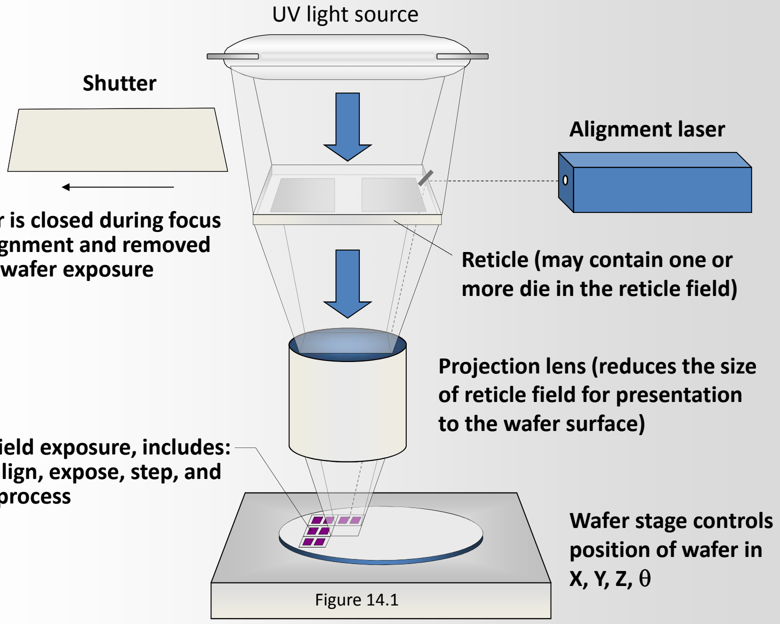
Pressure controller

Exhaust

Figure 10.16

Photolithography

Reticle Pattern Transfer to Resist



UV light source

Shutter

Alignment laser

Shutter is closed during focus and alignment and removed during wafer exposure

Reticle (may contain one or more die in the reticle field)

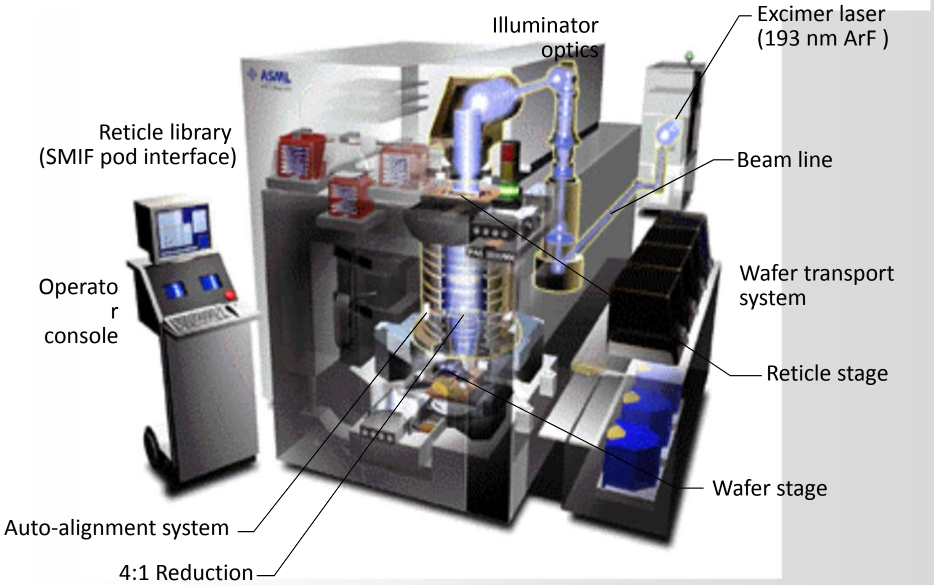
Projection lens (reduces the size of reticle field for presentation to the wafer surface)

Single field exposure, includes: focus, align, expose, step, and repeat process

Wafer stage controls position of wafer in X, Y, Z, θ

Figure 14.1

Step and Scan Exposure System



Illuminator optics

Excimer laser (193 nm ArF)

Reticle library (SMIF pod interface)

Beam line

Operator console

Wafer transport system

Reticle stage

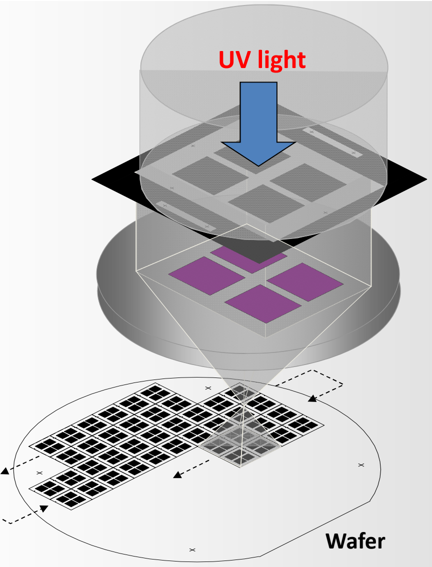
Wafer stage

Auto-alignment system

4:1 Reduction lens

NA = 0.45 to

Stepper Exposure Field



UV light

Reticle field size
20 mm × 15mm,
4 die per field

5:1 reduction lens

Image exposure on wafer
1/5 of reticle field
4 mm × 3 mm,
4 die per exposure

Serpentine stepping pattern

Wafer

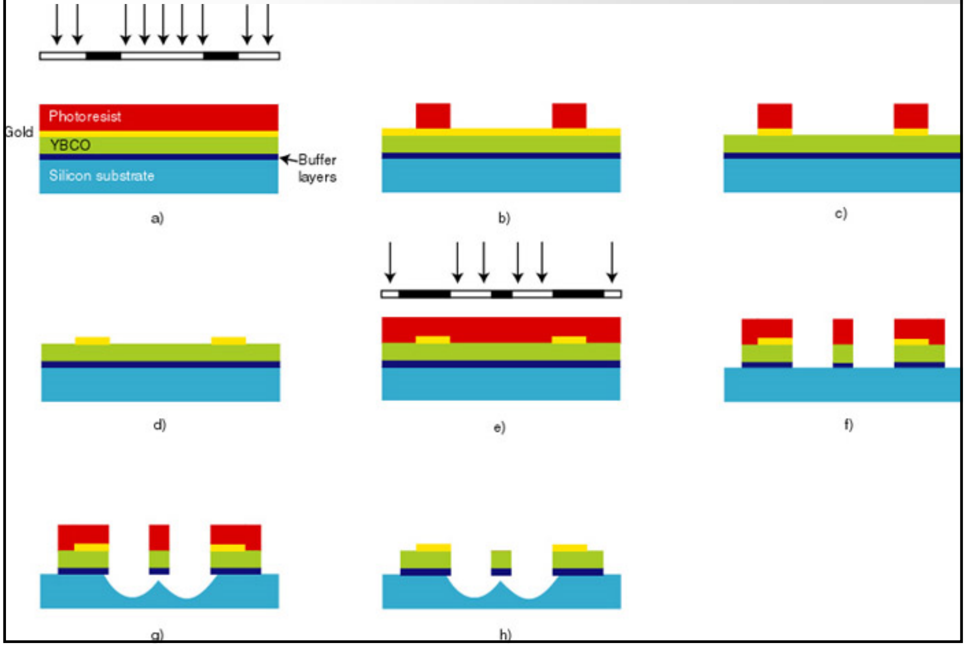
Photomask and Reticle for Microlithography

Photograph provided courtesy of Advanced Micro Devices

Photo 13.1

Etching

Schematic Flow

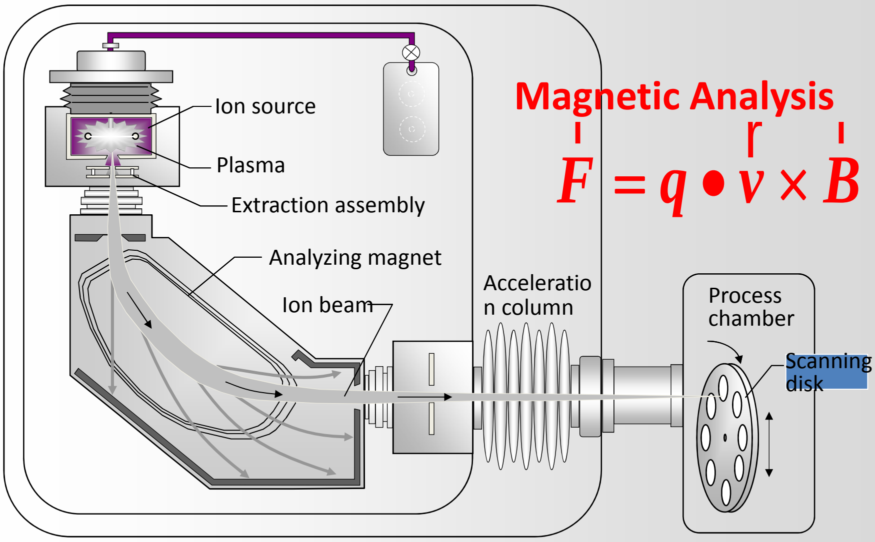


Wet Etching Station

A Typical Dry Etcher

Ion Implant

General Schematic of an Ion Implanter

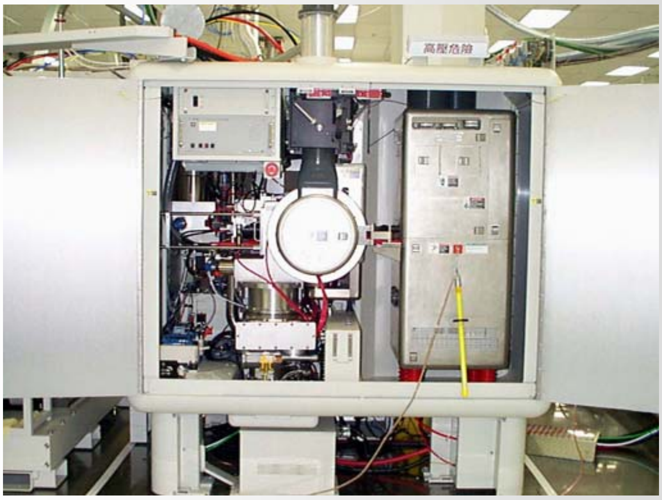


Magnetic Analysis

$$\vec{F} = q \bullet \vec{v} \times \vec{B}$$

Figure 17.6

Ion Implanter



Varian Semiconductor, VIISion 80 Source/Terminal side

Neutral Beam Trap

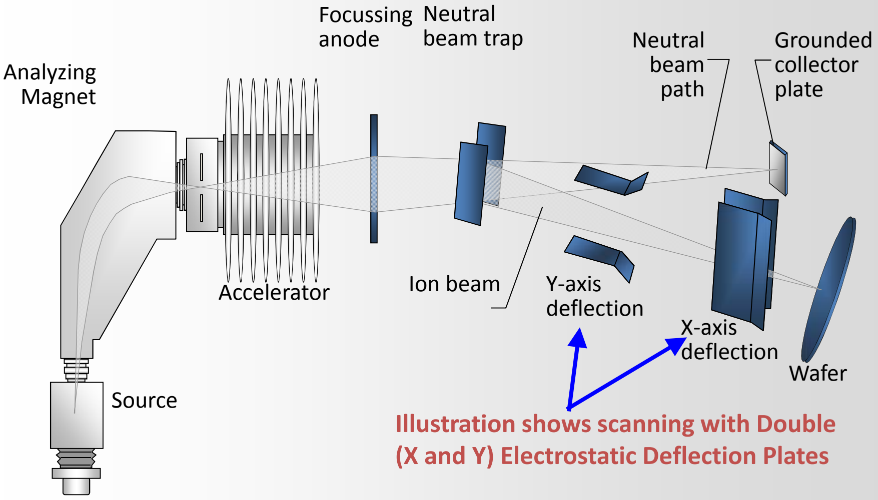


Illustration shows scanning with Double (X and Y) Electrostatic Deflection Plates

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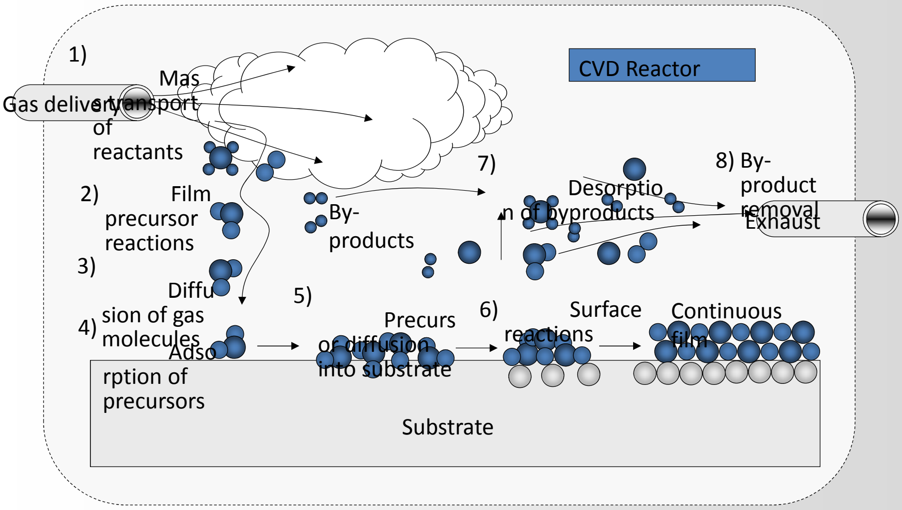
Thin Film Deposition

Schematic of CVD Transport and Reaction Steps



CVD Reactor

Gas delivery

1) Mass transport of reactants

2) Film precursor reactions

3) Diffusion of gas molecules

4) Adsorption of precursors

5) Precursor diffusion into substrate

6) Surface reactions

7) Desorption of byproducts

8) By-product removal

Exhaust

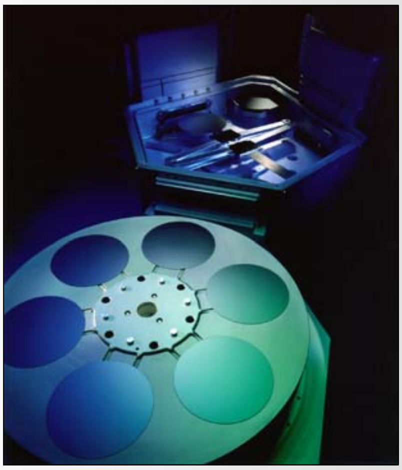
By-products

Continuous film

Substrate

Figure 11.8

Chemical Vapor Deposition Tool

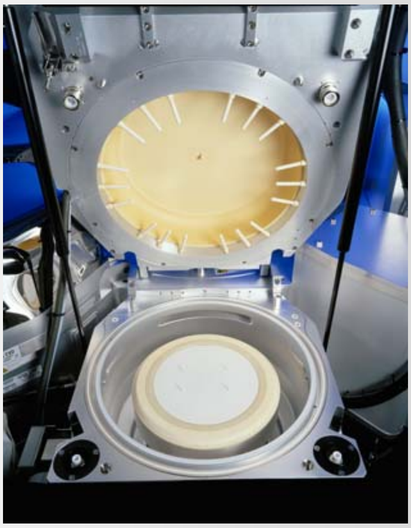


Photograph courtesy of Novellus, Sequel CVD

Photo 11.3

High Density Plasma Deposition Chamber

- Popular in mid-1990s
- High density plasma
- Highly directional due to wafer bias
- Fills high aspect ratio gaps
- Backside He cooling to relieve high thermal load
- Simultaneously deposits and etches film to prevent bread-loaf and key-hole effects

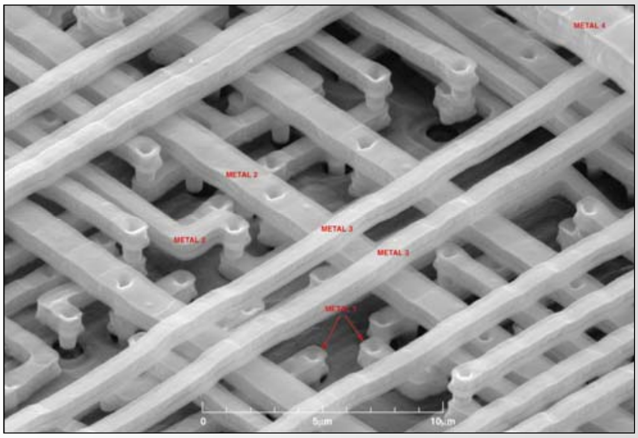


Photograph courtesy of Applied Materials, Ultima HDPCVD Centura

Photo 11.4

Metalization

Metal Layers in a Chip



Micrograph courtesy of Integrated Circuit Engineering

Photo 11.1

PVD Cluster Tool

Photo Courtesy of Applied Materials, Inc.

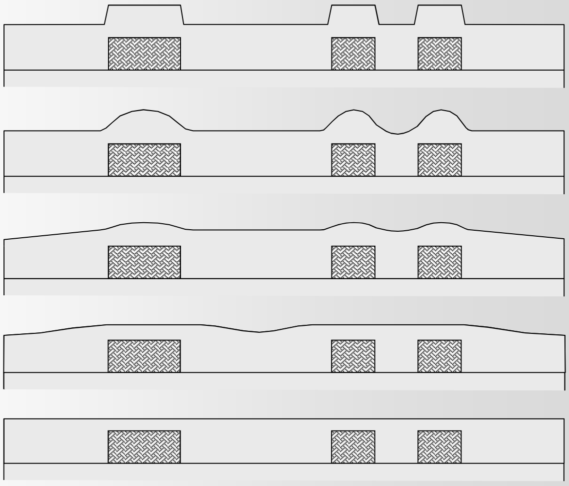
Photo 12.3

Electroplating Tool

Used with permission from Novellus Systems, Inc.
Photo 12.4

Polishing

Qualitative Definitions of Planarization



a) No planarization

b) Smoothing

c) Partial planarization

d) Local planarization

e) Global planarization

Figure 18.2

CMP Polishing Pad

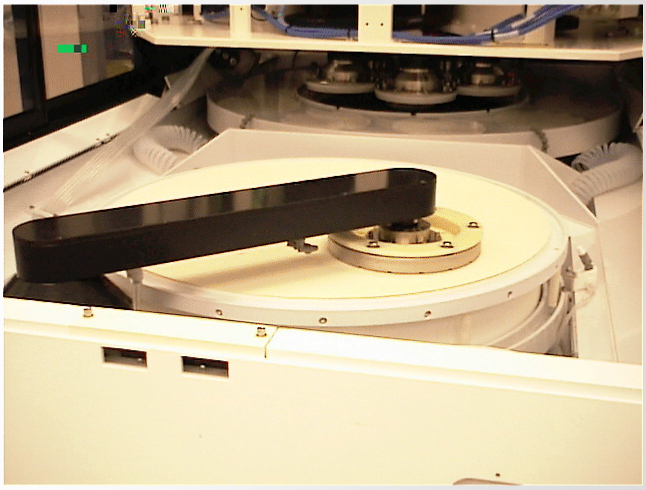
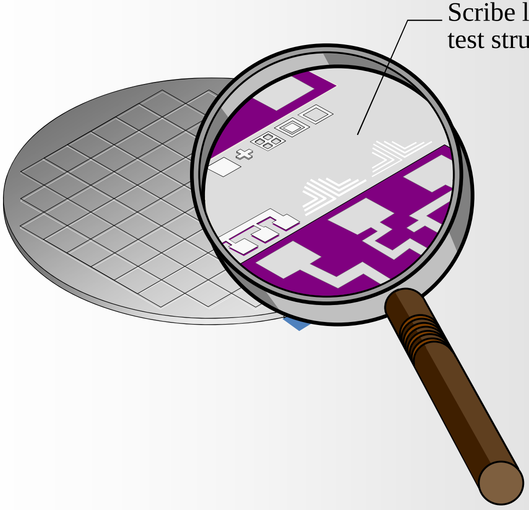


Photo courtesy of Speedfam-IPEC

Photo 18.2

Packaging

Scribe Line Monitor Test Structure



Scribe line with monitor
test structures

Figure 19.3

Traditional Assembly and Packaging

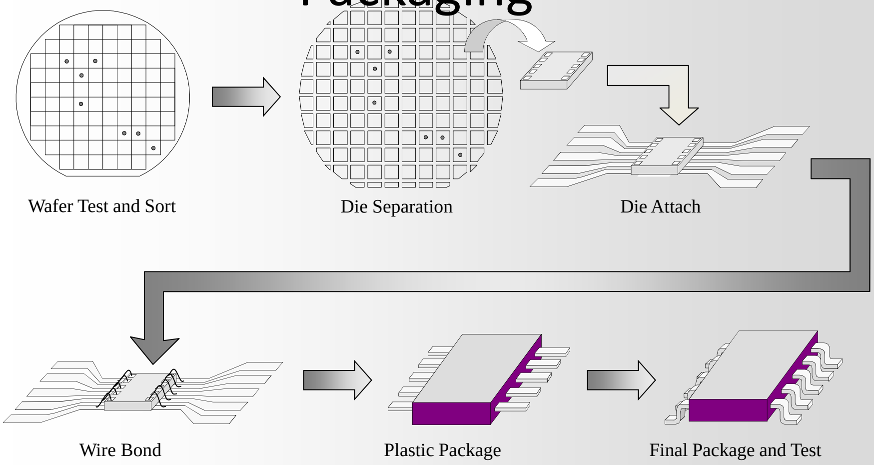
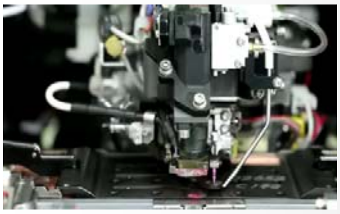


Figure 20.1

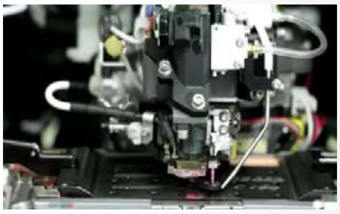
打線機 failure diagnostics

Z軸Flexure作動

Fast



Slow



1.打線過快會造成產品不穩定

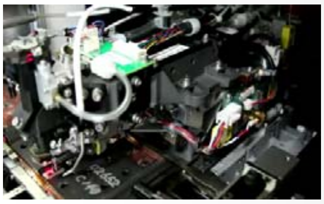
2.機構異常作業會有球型不良造成產品異常

透過Encoder以及顯微鏡來檢查

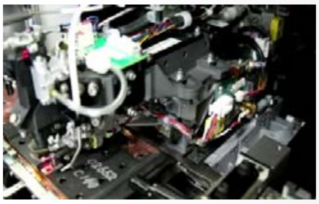
打線機 failure diagnostics

Table作業XY作動

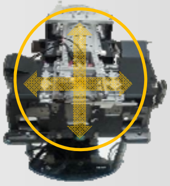
Fast



Slow



主要作動由XY軸線性馬達控制



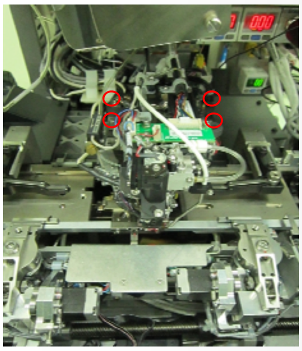
所以機構異常作業會有**球位偏**
造成產品異常

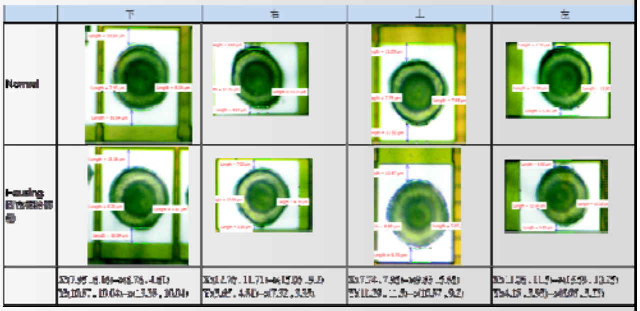
透過測力計以及Encoder來檢查

透過振動訊號的頻譜分析，推測出故障原因

打線機 failure diagnostics

將housing固定螺絲旋鬆模擬振動打INK觀察其品質差異



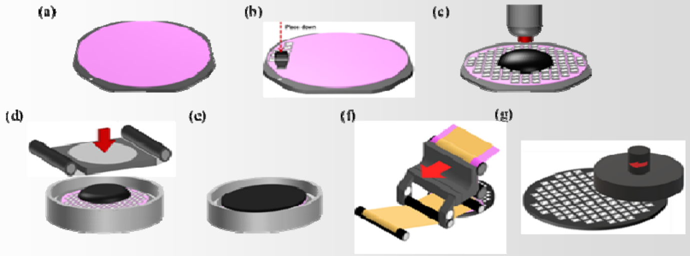


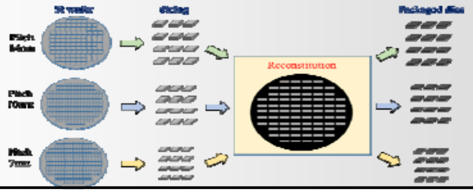
將housing固定螺絲旋鬆確實會造成球位偏

性能 ← 振動

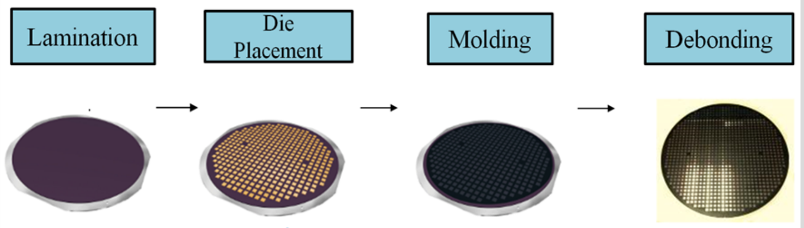
晶圓重組製程

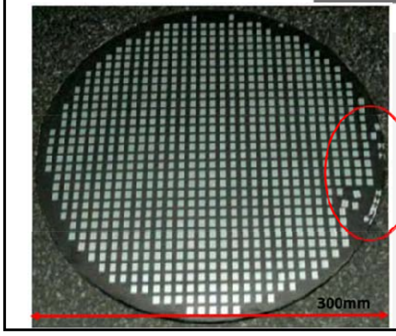
- 後段IC封裝技術為了趕上前段的發展速度，迎合不斷縮小的晶片尺寸與更多的IC接腳數，又須能夠以現有設備封裝不同大小的晶片尺寸，散出型重組製程以此需求為基礎，建立標準化的構裝流程，為連接半導體上下游技術的一段重要銜接製程。

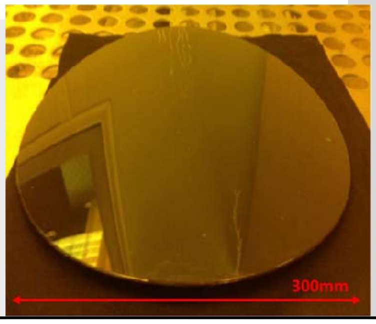




Recon Failure





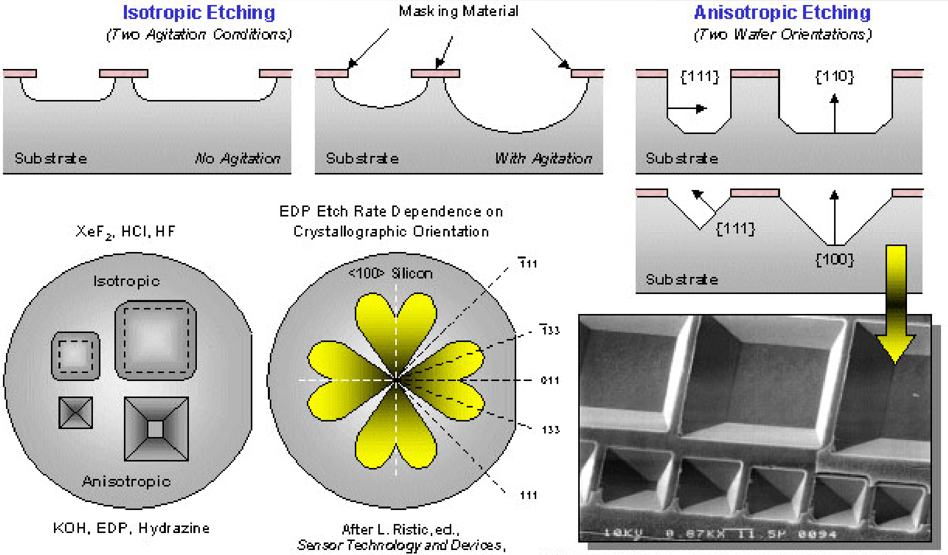


Part V. A Brief Introduction on Micro-Electro-Mechanical Systems (MEMS)

Bulk Micromachining

- Devices are shaped by etching a large single crystal substrate
- Thin films are used for isolation and transducer functions
- Anisotropic etching provide a high-resolution etch and tight dimensional control
- Bigger
- Waste of material
- Compatibility with IC process ?

Bulk Micromachining

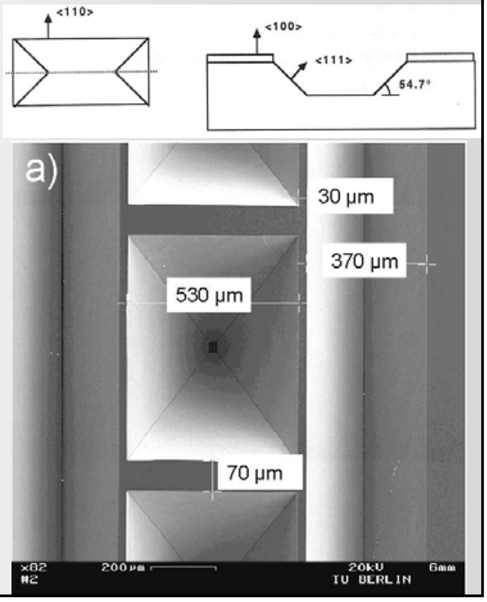


After L. Ristic, ed., *Sensor Technology and Devices*, Artech House, 1994.

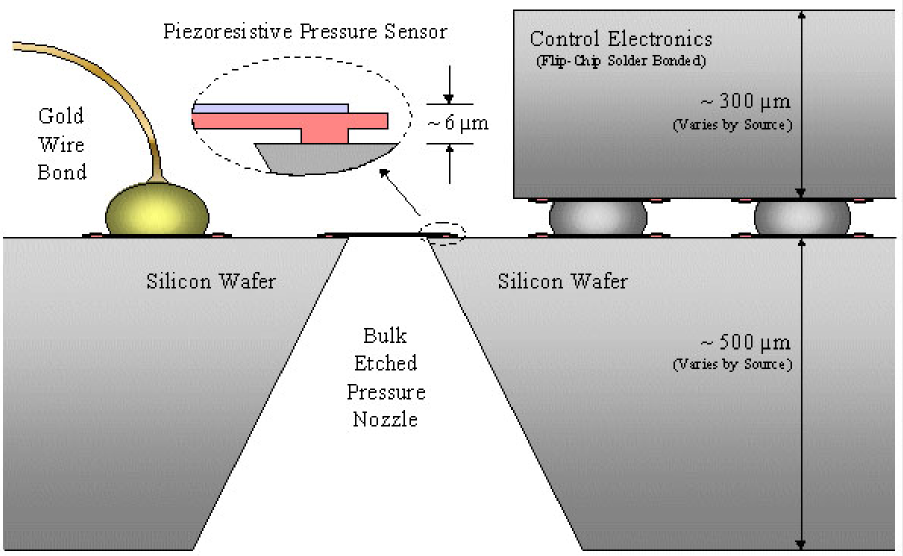
J. H. Comtois, Air Force Institute of Technology (AFIT), 1995.

Bulk Micromachining Technologies

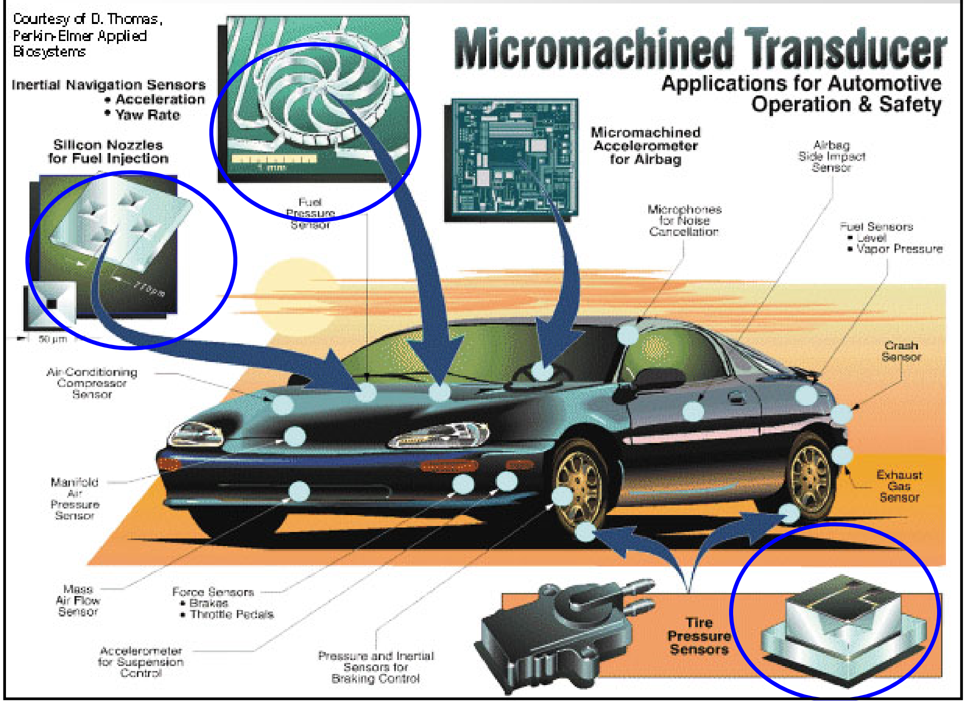
- Wet Anisotropic etch
  - KOH, EDP, Hydrazine, and TMAH exhibit crystalline orient dependent etch rate.
  - Widely used in traditional bulk micromachining for profile and dimension control



Bulk Micromachining: Definition

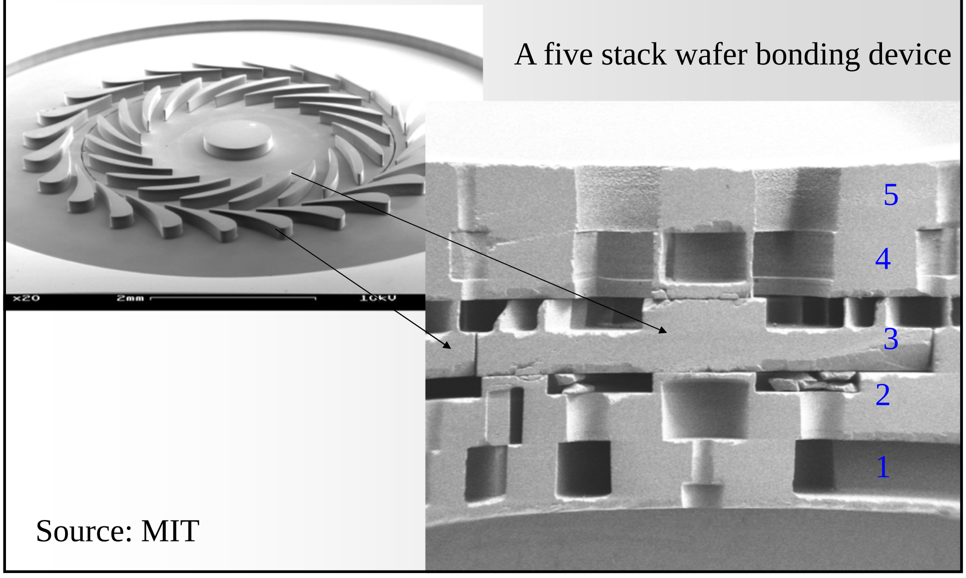


Courtesy of D. Thomas, Perkin-Elmer Applied Biosystems



Micro Engines

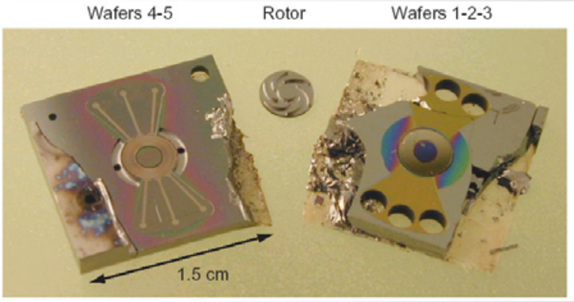
A five stack wafer bonding device



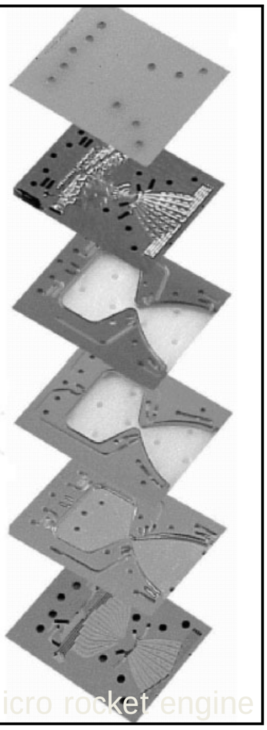
Source: MIT

Wafer Bonding Applications

- Good examples:
  - 20 stacks Du Pont micro reactors
  - 6 stacks micro rockets
  - 6 stacks micro compressors



Micro motor compressor



Micro rocket engine

Surface Micromachining

- Devices are built by thin films
  - Substrates are used as foundations
- Promise order of magnitude increase of device density
- Possible to integrate with build in electronics
- Thin film properties are highly sensitive to work in process

History of Surface Micromachining

- 1960‘s Nathanson et. al
  - Westinghouse research laboratory
  - Patterned metal film cantilever beam
- 1983 University of California at Berkeley
  - R. Howe, polysilicon micro structures
- 1985 Barth
  - Define “surface micromachining”
- 1989 Fan, Tai, Muller
  - micromotors

Common Surface Micromachining Processes

- Thin film deposition
  - – Either by CVD or PVD method to form thin film structures
- Patterning of structures
  - – Lithpgraphy process
- Thin film etch
  - – Either by wet or dry etch to form the shape of structures and remove sacrificial layers

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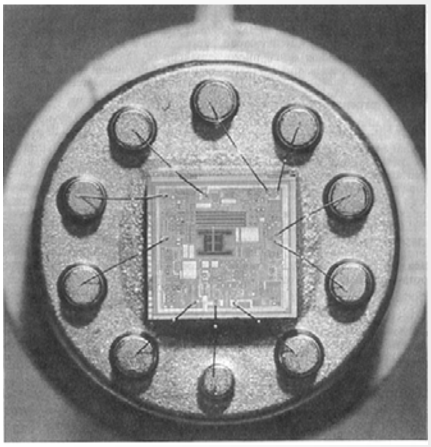
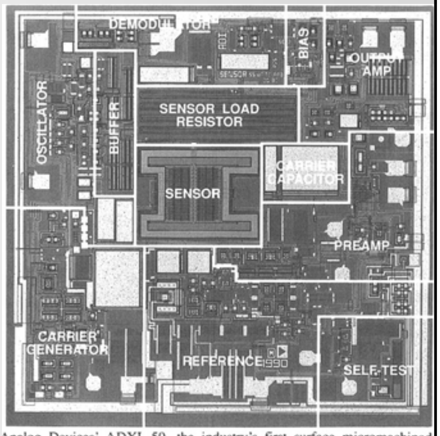
CMOS-MEMS Integration



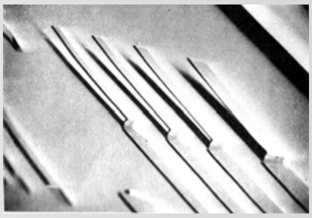


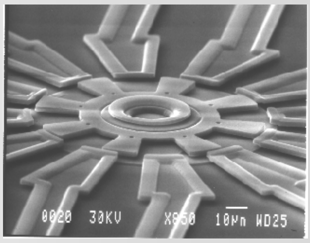
Analog Devices' ADXL-50, the industry's first surface micromachined accelerometer, includes signal conditioning on chip.

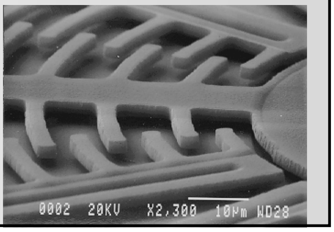
Analog Device, ADXL-50 surface machined accelerometers

Surface Micromached Examples

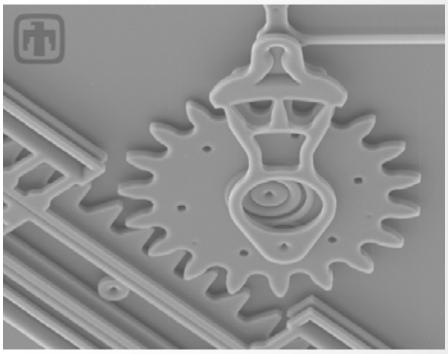
- Cantilever beams
  - The most common MEMS structures
  - Have used in accelerometers, pressure sensors, pumps, etc.
- Micro motors
  - The most well-known micromachined devices in the early MEMS development
- Comb drives
  - The most important MEMS actuators

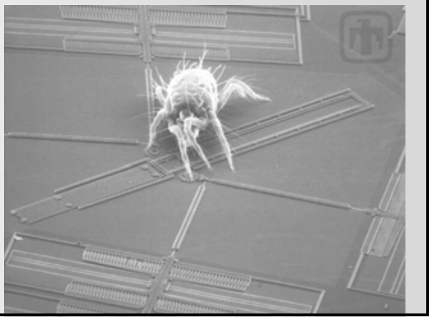




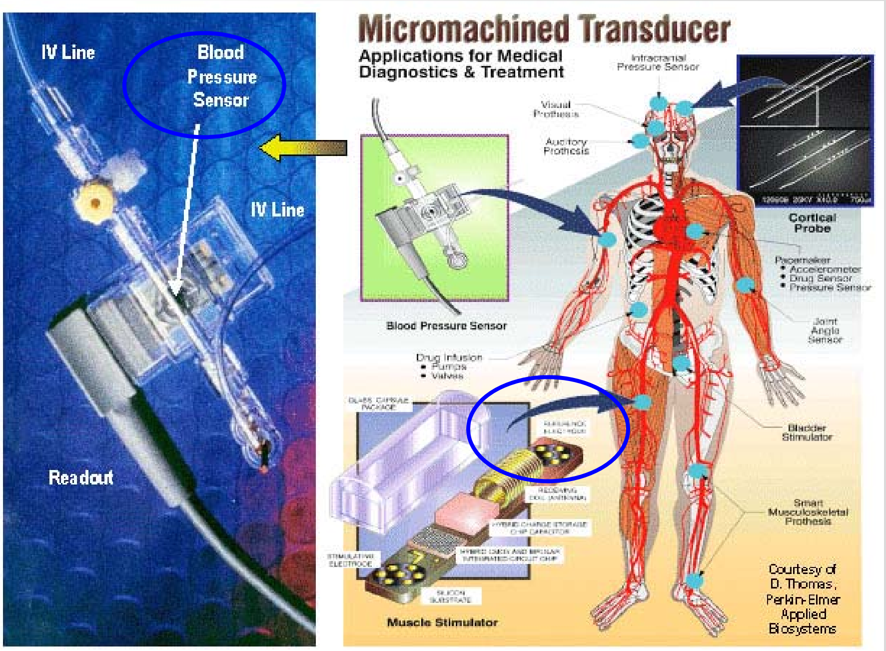


Surface Micromachined Applications





- Sandia Nat'l Lab's optical bench
  - Its own standard process
  - Combining gear, hinge, comb drives, etc



Courtesy of D. Thomas, Perkin-Elmer Applied Biosystems

The END